ISSN XXXX XXXX © 2019 IJESC

Research Article Volume 9 Issue No.3

A 10-T SRAM Cell with Inbuilt Charge Sharing for Dynamic Power Reduction

Akila. P[1], Saranya. K[2], Ramesh. V[3]
UG Student[1, 2], Assistant Professor[3]
Department of Electronics and Communication Engineering
Jeppiaar SRR Engineering College,Tamil Nadu, India

Abstract:
As microprocessors and other electronics applications get faster and faster, the need for large quantities of data at very high speeds increases, while providing the data at such high speeds gets more difficult to accomplish. As microprocessor speeds increase from 25 MHz to 100 MHz, to 250 MHz and beyond, systems designers have become more creative in their use of cache memory, interleaving, burst mode and other high-speed methods for accessing memory. There are many reasons to use an SRAM or a DRAM in a system design. Design tradeoffs include density, speed, volatility, cost, and features. All of these factors should be considered before you select a RAM for your system design. Fast, synchronous SRAMs can operate at processor speeds of 250 MHz and beyond, with access and cycle times equal to the clock cycle used by the microprocessor. A novel 10T SRAM cell design with an inbuilt mechanism for charge recycling to cut down the dynamic power budget. The read discharge power of a single ended 8T cell is reused efficiently in the proposed cell architecture. The proposed design is built after analyzing the different types of SRAM using low power design techniques the simulations were done under DSCH & Microwind Software.

Keywords: DSCH, High Frequency, Power Reduction, SRAM, Microwind Software, Verilog Code.

I. INTRODUCTION

Static random- access memory (SRAM) is a type of semiconductor memory where the word static indicates that, unlike dynamic RAM (DRAM), it does not need to be periodically refreshed, as SRAM uses bistable latching circuitry to store each bit. SRAM exhibits data remanance, but is still volatile in the conventional sense that data is eventually lost when the memory is not powered. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFET so store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, 10T, or more transistors per bit. This is sometimes used to implement more than one (read and/or write) port, which may be useful in certain types of video memory and register files implemented with multi-ported SRAM circuitry. Generally, the fewer transistors needed per cell, the smaller each cell can be. Since the cost of processing silicon wafer is relatively fixed, using smaller cells and so packing more bits on one wafer reduces the cost per bit of memory. Memory cells that use fewer than 6 transistors are possible but such 3T or 1T cells are DRAM, not SRAM (even the so-called 1T-SRAM).Access to the cell is enabled by the word line which controls the two access transistors M_5 and M_6 which in turn, control whether the cell should be connected to the bit lines BL and BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins. During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs in a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bitline to swing upwards or downwards. The symmetric structure of SRAMs also allows for differential signaling, which makes small voltage swings more easily detectable. Another difference with DRAM that contributes to making SRAM faster is that commercial chips accept all address bits at a time. By comparison, commodity DRAMs have the address multiplexed in two halves, i.e. higher bits followed by lower bits, over the same package pins in order to keep their size and cost down. The size of an SRAM with *m* address lines and *n* data lines is 2^m words, or $2^m \times n$ bits.

II. SRAM CELL WITH NM TECHNOLOGY

Cell stability and area are among the major concerns in SRAM cell designs. This paper compares the performance of the four SRAM cell topologies, which include the conventional 6T-cell and the recently published 8T, 9T & 10T-cell implementations. To overcome the problem of data storage destruction during the read operation, an 8T-cell implementation was proposed, for which separate read/write bit and word signal lines are used to separate the data retention element and the data output element. In turn, the cell implementation provides a read-disturb-free operation. However, this implementation uses eight transistors, which results in a cell area increase of 30% in comparison to the conventional 6T-cell design. The efficiency of the 9T SRAM cell is enhanced by designing it to work with lower supply voltages, which helps in further reduction of the leakage power. The power consumption in 10T SRAM cell has 0.198mw; it is less compared to the other 9T SRAM Cell. In particular, the static-noise-margin (SNM) of each cell design and frequency, height, width, surf variation is examined.

There are 4types of SRAM Cell architecture, i.e

- 6T-Cell SRAM
- 8T-Cell SRAM
- 9T-Cell SRAM
- 10T-Cell SRAM

III. 6T-CELL DESIGN

The most commonly used SRAM cell implementation has the advantage of low static power dissipation. In any design using on-die cache, the 6T SRAM cell is the most frequently used cell. The main functionality of the 6T SRAM cell is to store data. SRAM cell design involves a complex balance a number of factor, some of which include:

- Minimize cell area to achieve high density,
- Reduce power and cost.
- Cell stability to prevent yield loss due to data corruption.
- Minimize supply voltage in order to reduce power. Good soft error immunity.
- High cell read current to minimize access time.
- Minimize word line pulse width to save on power by reducing bitline swing
- Minimize leakage current, especially for battery operated systems.

Many of these SRAM design factors are conflicting in nature. For example, good cell stability, small access time, and good soft error immunity would benefit from using larger transistors, but larger transistors would result in larger area and increased leakage.

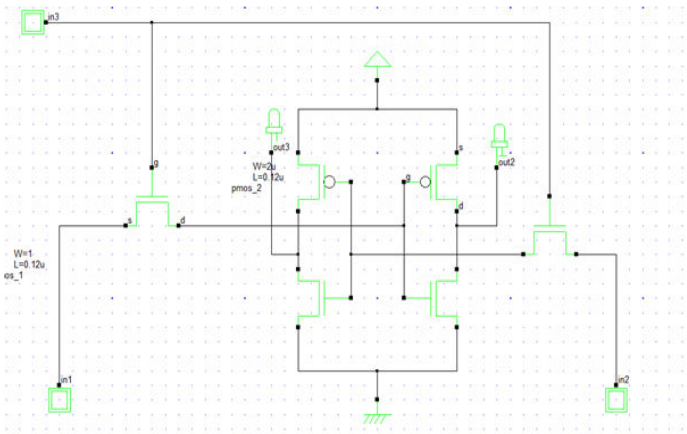

Figure .1.the schematic of conventional 6T SRAM cell.

For proper writing operation, one bit line is high and the other bit line is low. For writing "0", BL is low and BL bar is high. When the word line (WL) is asserted high, both access transistors T2 and T5 are turned ON and any charge which is stored in the BL goes through T2-T3 path to ground. Due to zero value on Q bar, the transistor T4 is ON and T6 is OFF. So the charge is stored at Q bar line. Similarly in the write "1" operation, BL is high and BL bar is low, due to this T6 is ON and the charge stored on Q bar is discharged through the T5-T6 path and due to this low value on the Q bar , T1 is ON and T3 is OFF, so the charge is stored on the Q. Before the read operation of "1" at Q (for example) begins, BL and BL bar are pre-charged to as high as Vdd. When the WL is selected, the access transistors T2 and T5 are turned ON. Because of the pull-up transistor T1 ON and pull down transistor T3 OFF, voltage of BL will be nearly Vdd. On the other side, current will flow from the pre-charged BL bar to ground, thus discharging BL bar line through T5-T6 path to ground; T4 being OFF. Thus, a differential voltage develops between BL and BL bar lines. This small potential difference between the bit lines is sensed and amplified by the sense amplifier at the data output. To overcome the problem of data storage destruction during the read operation, an 8T-cell implementation was proposed, for which separate read/write bit and word signal lines are used to separate the data retention element and the data output element. In turn, the cell implementation provides a read-disturb-free operation. However, this implementation uses eight transistors, which results in a cell area increase of 30% in comparison to the conventional 6T-cell design.

IV. 8T-CELL DESIGN

Negative Bias Temperature Instability (NBTI) is a well known reliability concern for PMOS transistors. We review the literature to find seven key experimental features of NBTI degradation. These features appear mutually inconsistent have often defied easy interpretation. By reformulating the Reaction-Diffusion model in a particularly simple form, we show that these seven apparently contradictory features reflect different facets of the same underlying physical of NBTI actually mechanism. Basically this new single ended 8T SRAM cell consists of an inverter which replaces the two ground of the SRAM cell. So in the ideal stage (where there is no data) the power leakage in the PMOS is reduced considerably by the use of the invertors. The PMOS transistor is negatively biased for certain period of time which is also called as stress mode. The interface traps are eliminated by applying of input log"1"to the gate terminal (Vgs=0). In this paper we are going to tackle this NBTI problem by increasing the recovery time. This method is called as recovery boosting and it is valid only when the data is considered as invalid. During the normal mode of operation the inverter has an input has a value"1"which in turn consider the value as output"0" that is taken as ground. The ground voltage node is raised as the input has an output "1" of the SRAM cell.

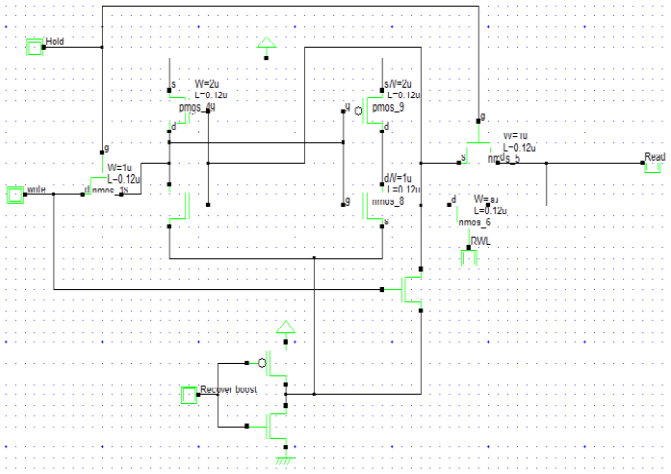

Figure.2. the Schematic of Conventional 8T SRAM cell.

V. 9T-CELL DESIGN

For simultaneously reducing leakage power and enhancing data stability a 9T SRAM cell is used. In a 9T SRAM cell the data is completely isolated from the bit lines during a read operation. The read SNM of such circuit is thereby enhanced as compared to a conventional 6T SRAM cell. In an idle 9T SRAM cell, the cells are placed into a super cut-off sleep mode, thereby reducing the leakage power consumption. However in case of SRAM, switching OFF the circuit does mean losing the data, and unfortunately it is a compulsion to keep the cell ON even in the idle state. This situation is a major challenge in reducing the leakage current as we have no option but to keep the circuit ON. To overcome the limitations

mentioned above, the proposed SRAM cell has been designed with a different read process which reduces the time required to read the cell and also reduces the chance of data corruption of cell by isolating it from the external read circuitry.The efficiency of the cell is enhanced by designing it to work with lower supply voltages, which helps in further reduction of the leakage power.

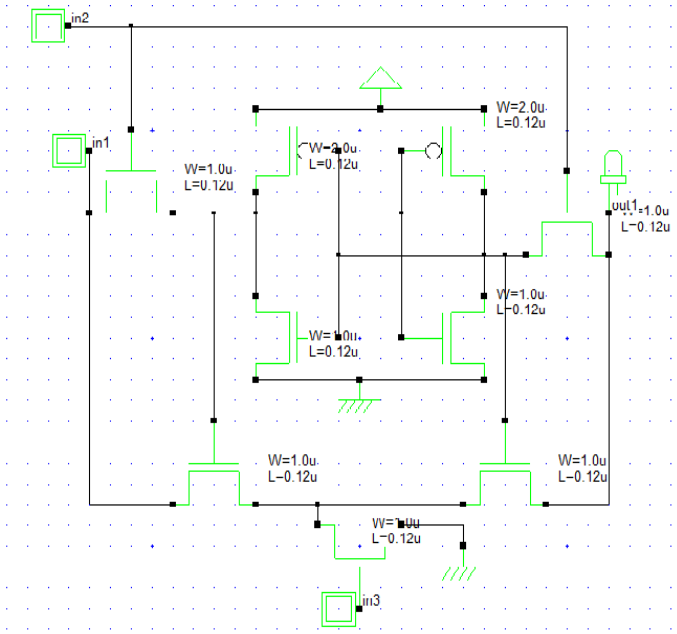

Figure .3. The Schematic of 9T SRAM cell

VI. 10T-CELL DESIGN

Designing a SRAM cell in nano scale regime has become a challenging task because of reduction in noise margins and increased sensitivity to threshold voltage variation. 10T SRAM cell performs better then 6T SRAM cell in terms of reliability and stability. 6T SRAM cell has less reliability at low supply voltage due to degradation in noise margins The architecture of a 10T SRAM cell is similar to the 6T SRAM cell except additional read circuitry Fig. 2 shows the designed 10T SRAM cell. In this 10T SRAM cell, 10 transistors have been used. It consists of conventional 6T SRAM cell and an additional read circuitry. Difficulty in conventional 6T SRAM cell is the high risk of data loss during read operations. There is possibility of flipping node voltage at Q and Q' due to back to back inverter actions. This situation can be avoided using extra read circuitry. In this 10T SRAM cell, write operation is same as in 6T SRAM cell [6-7]. In case of read operation, charge sharing takes place between read bit line (RBL) and uncharged bit line BL / BLB during read operation. Due to sharing of charge, read bit line does not discharge completely and stay at mid voltage level. Hence this cell behaves as an automatic bit line swing limiter. The proposed circuit is given best result in reducing average power consumption during write operation, with activating the WWL and giving a high input to bit line. As the bit line and bit bar lines are added with an inverter, so it will generate the complementary date automatically when any one of the bit line is selecting in accordance to circuit operation need. The average power consumption is calculated by micro wind 3 used for designing and simulating the proposed SRAM cell circuits at layout level by selecting the foundry value for this proposed SRAM cell is 0.6µm CMOS technology and after that choosing the appropriate cell ratio, for PMOS it is W\L = 2.00/0.12 and for NMOS its value is taken W/L = 1.00/ 0.12. The cell ratio is very important factor in SRAM cell in term of data stability during read and writes operation the proposed SRAM cell is more focused on reduction in power consumption during write operation by using dual word line approach, using two separated word line for write (WWL) and read (RWL) operation. The SRAM with 0.6µm technology, the average write power consumption is being reduced with the help of the two transistors used in pull down network of latch and the bit line and bit bar line are cross coupled with these two tail transistors is responsible reduce the number of times to charge and discharge the large bit lines capacitance to reduce the write power consumption. The proposed SRAM circuit is designed at layout level and when simulation is performed then by default voltage Vs time curve is generated and the average power consumption is automatically calculated in microwind simulator tool.

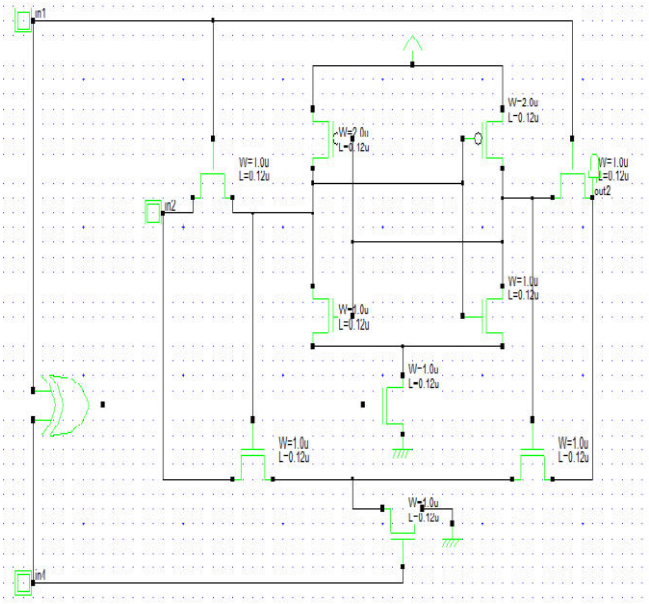

Figure .4.The Schematic of 10T SRAM Cell

This total average write power consumption of proposed SRAM cell is compared with conventional 6T SRAM cell as for showing the actual reduction in power consumption in proposed SRAM cell.

VII. SIMULATION RESULTS

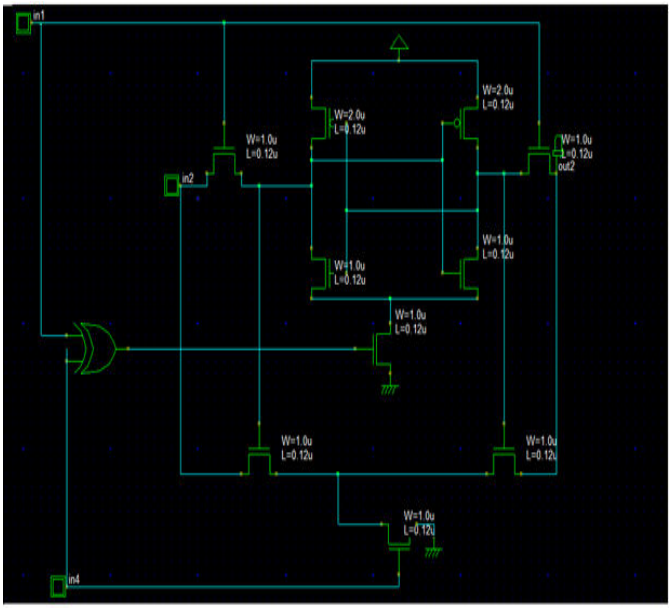

Figure .5. A Novel Schematic Diagram of 10-T Cell

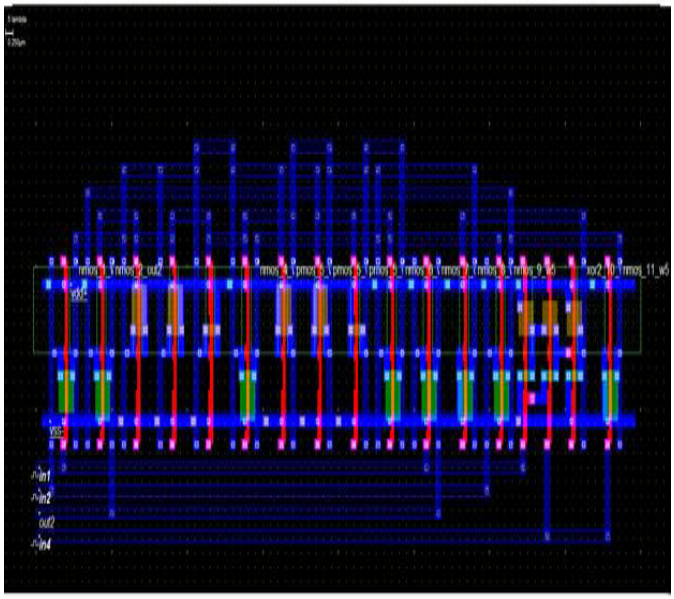

Figure. 6.a novel column of 10-T cell layout diagram.

ANALOG SIMULATION OF 6T 8TAND 10T

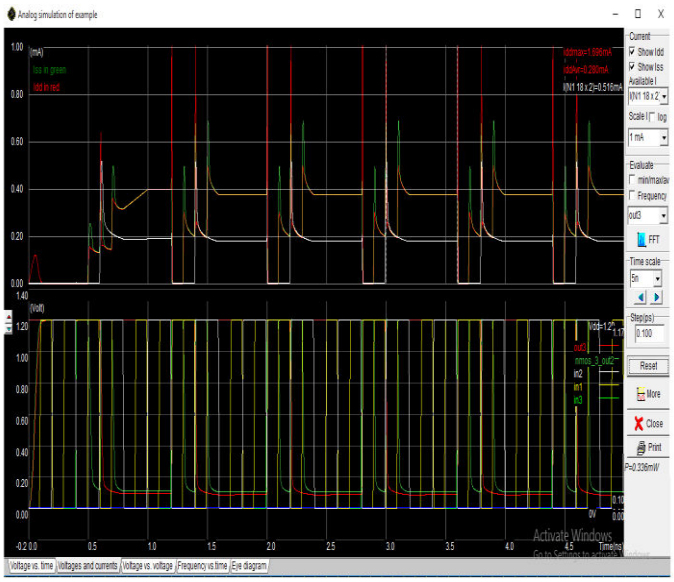

Figure .7.Waveform of Voltage Vs Current Of 6t.

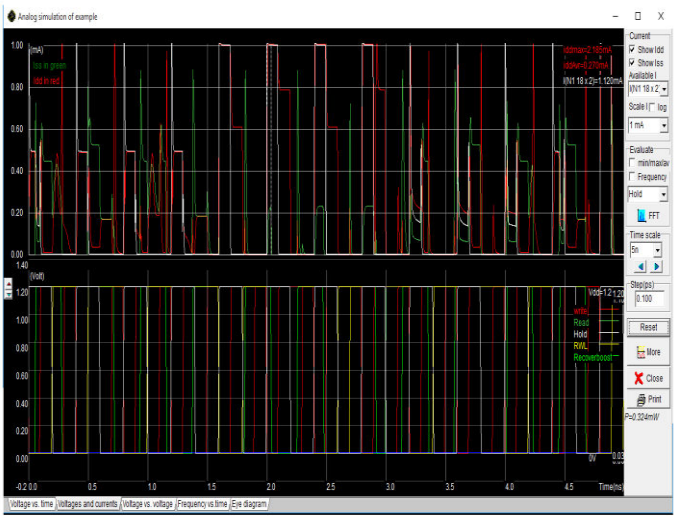

Figure. 8.Waveform of Voltage Vs Current.

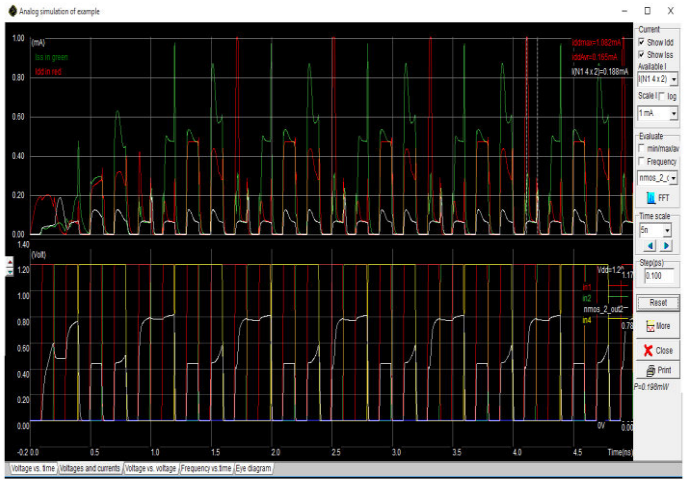

Figure. 9.waveform of voltage vs current.

VIII. OUTPUT COMPARISON TABLE

Table. I.Power Consumption Table

Sl.No	BIT CELL TOPOLOGIES	POWER CONSUMPTION
1	6-T SRAM bitcell	0.336 mw
2	8-T SRAM bitcell	0.324 mw
3	9-T SRAM bitcell	0.242 mw
4	10-T SRAM bitcell	0.198 mw

Table.2. Comparison of frequency.

Sl.No	BIT CELL TOPOLOGIES	FREQUENCY (GHz)
1	6-T SRAM bitcell	1.25
2	8-T SRAM bitcell	2.50
3	9-T SRAM bitcell	3.75
4	10-T SRAM bitcell	7.32

IX. ADVANTAGES AND DISADVANTAGES

ADVANTAGES:

1. Power consumption is reduced comparison to ST-1 and ST-2 bit cell. The power consumption is 3.642µw. Hence low power.
2. No power distortion.
3. Low area, 2X area will be reduced comparison to 10T and ST-2 bit cell.
4. Low density and low efficiency.
5. High speed accessing memory.

DISADVANTAGES:

1. High cost.
2. Two word lines are used for data reading.
3. Virtual ground effect for high power transistor.

X. APPLICATIONS

- In future mobile Systems and core processors for low leakage & enhanced battery efficiency.
- Future Integrated circuits for low power and high speed applications using power gated circuits.

XI. CONCLUSION

We studied a novel 10T-CDC column-decoupled SRAM design. The half-select free design enables enhanced voltage

Scaling capabilities and 30%–40% power reduction in comparison to standard 6T techniques. This study involved a 90-nm read assist-based sense Amp design, and a 65-nm domino read-based design with dynamic supply capabilities. The 10T-CDC cell enables significant power savings in terms of reduction for read-assist design, and half-select column power reduction in dynamic dual supply domino read designs with the aid of new header designs. New simplified local evaluation logic and shorter bitlines are employed for the domino read-based design. Simulations showed high performance for the proposed design using shorter bit lines and dynamic header circuit. Measured hardware data from fabricated chips in 90- and 65-nm PD/SOI technology shows improved stability and yield, and voltage scalability due to the elimination of half-select disturb with comparable access times as that of 6T-based designs.

XII. REFERENCES

[1]. Bo, Z., et al. (2007) 'A Sub-200mV 6T SRAM in 0.13um CMOS'. In Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International.

[2]. Brown, A.R., Roy, G., and Asenov, (2007) 'A Poly-Si-Gate- Related Variability in Decananometer MOSFETs With Conventional Architecture'. Electron Devices, IEEE Vol. 54(11), pp. 3056-3063.

[3]. Chang, L., et al., (2008) 'An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High-Performance Caches'. Solid-State Circuits, IEEE Journal of, Vol. **43**(4), pp. 956-963.

[4]. Cheng, B., Roy, S., Roy, G., Brown, A., and Asenov, (2006) 'A. Impact of Random Dopant Fluctuation on Bulk CMOS 6-T SRAM Scaling'. In Solid-State Device Research Conference, ESSDERC.

[5]. Jawar Singh, D.K.P., Simon Hollis, and Saraju P, Mohanty , (2008) 'A single Ended 6T SRAM Cell Design for Ultra-Low-Voltage Applications'. IEICE Electronics Express Vol.**5**(18), pp. 750-755.

[6]. Kevin, Z., (2009) 'Embedded Memories for Nano-Scale VLSIs'. Springer Publishing Company Incorporated 400.

[7]. Mizuno, H. and T. Nagano, (1996) 'Driving Source-Line Cell Architecture for Sub-1-V High-Speed Low-Power Applications'. Solid-State Circuits, IEEE Journal Vol.**31** (4), pp. 552-557.

[8]. Tae-Hyoung, K., et al. (2007) 'A High-Density Sub threshold SRAM with Data-Independent Bitline Leakage and Virtual Ground Replica Scheme'. In Solid-State Circuits Conference, ISSCC. Digest of Technical Papers, IEEE International.

[9]. Takeda, K., et al.,(2006) ' A Read-Static-Noise-Margin-Free SRAM Cell For Low-VDD and High-Speed Applications Solid-State Circuits, IEEE Journal of, Vol.**41** (1) , pp. 113-121.

[10]. Wang, X., Roy, S., and Asenov, (2009) ' A Impact of Strain on the Performance of high-k/metal Replacement Gate MOSFETs', in Proc. 10th Ultimate Integration on Silicon (ULIS).