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Design of Double-Tail Comparator in 90nm Technology

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Abstract:
The need for extremely-low-strength, place efficient and excessive velocity analog-to-virtual converters is pushing towards using dynamic regenerative comparators to maximize velocity and electricity efficiency. In this paper, a new dynamic comparator is proposed, where in the circuit of a conventional double-tail comparator is modified for low-strength and rapid operation even in small deliver voltages. Without complicating the layout and by using adding few transistors, the nice feedback for the duration of the regeneration is reinforced, which leads to remarkably decreased delay time. It is shown that within the proposed dynamic comparator both the power intake and delay time are considerably decreased. The most clock frequency of the proposed comparator may be increased to 2.5 and 1.1 GHz at deliver voltages of 1.2 and zero.6 V, even as eating 1.4 mW and 145 µW, respectively. The same old deviation of the input-referred offset is 7.8 mV at 1.2 V supply. All of the circuits designed in gpdk 90nm generation with the usage of cadence tool

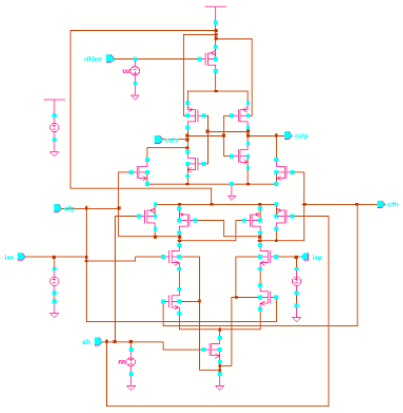
Keywords: ultra-low-power, double-tail comparator, positive feedback, delay time, cadence tool.

I. INTRODUCTION

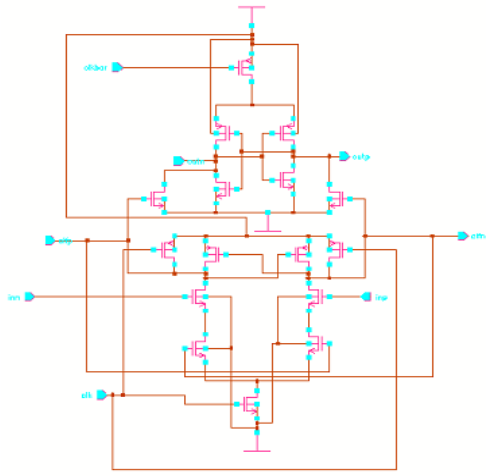
COMPARATOR is one of the essential constructing blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require excessive-pace, low strength comparators with small chip location. Excessive-pace comparators in ultra-deep sub micrometer (u.s.) CMOS technology suffer from low supply voltages especially whilst considering the reality that threshold voltages of the gadgets have not been scaled on the same pace as the deliver voltages of the present day CMOS approaches. Consequently, designing high-velocity comparators is tougher when the supply voltage is smaller [1]. In other phrases, in a given generation, to reap high pace, larger transistors are required to compensate the discount of deliver voltage, which additionally approach that more die region and electricity is wanted. except, low-voltage operation outcomes in confined common-mode enter variety, which is important in lots of high-pace ADC architectures, which includes flash ADCs [6]. Many techniques, such as supply boosting methods, techniques employing body-driven transistors, current-mode design and those using dual-oxide processes, which can handle higher Supply voltages were evolved to satisfy the low-voltage design demanding situations. Boosting and bootstrapping are strategies based totally on augmenting the supply, reference or clock voltage to deal with input-range and switching problems [3]. Those are powerful techniques, but they introduce reliability troubles specifically in use CMOS technologies. Body-pushed method followed with the aid of Blalock, removes the brink voltage requirement such that frame driven MOSFET operates as a depletion-type device. Based on this technique, a 1-bit quantize for sub-1V modulators is proposed. Despite the blessings, the frame pushed transistor suffers from smaller Trans conductance compared to its gate-pushed counterpart even as unique fabrication system, consisting of deep n-well is needed to have each n-MOS and p-MOS transistors perform inside the frame-driven configuration here, a comprehensive evaluation approximately the delay of dynamic comparators has been offered for numerous architectures. Furthermore, primarily based at the double-tail shape proposed in, a new dynamic comparator is presented, which does now not require boosted voltage or stacking of too many transistors. Merely through adding some minimum-size transistors to the conventional double-tail dynamic comparator, latch postpone time is profoundly decreased. This transformation additionally consequences in widespread energy financial savings when compared to the conventional dynamic comparator and double-tail comparator.

II.DOUBLE-TAIL DYNAMIC COMPARATOR

The schematic diagram of the proposed dynamic double-tail comparator is demonstrated in fig 1.Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase △Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner [8].



(a) Main idea.



(b) Final structure.

Figure.1.Schematic diagram of the proposed dynamic comparator.

III.OPERATION OF THE PROPOSED COMPARATOR

The operation of the proposed comparator is as follows. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground.

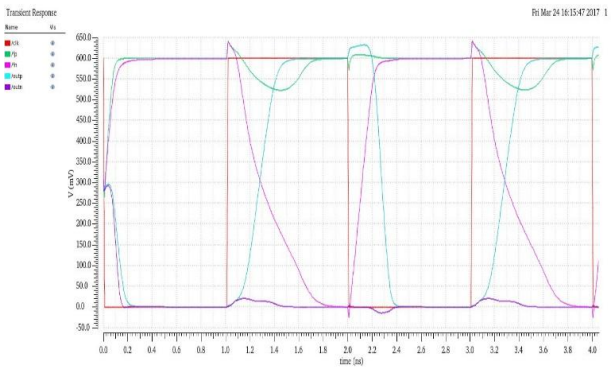


Figure.2. Transient simulations of the proposed double-tail dynamic comparator

During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which $\triangle$Vfn/fp is just a function of input transistor transconductance and input voltage difference (9), in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp ($\triangle$Vfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [Msw1 and Msw2 as shown]. At the start of the choice making section, due to the truth that both fn and fp nodes were pre-charged to VDD (in the course of the reset phase), both switches are closed and fn and fp begin to drop with different discharging fees. As quickly as the comparator detects that one of the fn/fp nodes is discharging faster, manage transistors will act in a way to growth their voltage difference. assume that fp is pulling as much as the VDD and fn must be discharged completely, as a result the switch inside the charging route of fp could be opened (so as to prevent any modern drawn from VDD) however the other switch connected to fn may be closed to allow the whole discharge of fn node. In different words, the operation of the manipulate transistors with the switches emulates the operation of the latch. This can be more mentioned within the following section.

IV.DESIGN CONSIDERATIONS

In designing the proposed comparator, some design issues must be considered. When determining the size of tail transistors (Mtail1 and Mtail2), it is necessary to ensure that the time it takes that one of the control transistors turns on must be smaller than t0 (start of regeneration)

$$t_{on,Mc1(2)} < t_0 \rightarrow \frac{|V_{Thp}| \cdot C_{L,fn(p)}}{I_{n1,2}} < \frac{V_{Thn} C_{Lout}}{I_{B1}}$$
$$\rightarrow \frac{|V_{Thp}| \cdot C_{L,fn(p)}}{\frac{I_{Tail1}}{2}} < \frac{V_{Thn} \cdot C_{Lout}}{\frac{I_{Tail2}}{2}}.$$

This condition can be easily achieved by properly designing the first and second stage tail currents. Even if possible in the fabrication technology, low-threshold pMOS devices can be used as control transistors leading to faster turn on. In designing the nMOS switches, located below the input transistors, the drain-source voltage of these switches must be considered since it might limit the voltage headroom, restricting the advantage of being used in low-voltage applications. In order to diminish this effect, low-on-resistance nMOS switches are required. In other words, large transistors must be used. Since the parasitic capacitances of these switches do not affect the parasitic capacitances of the fn/fp nodes (delay bottlenecks), it is possible to optimally select the size of the n-MOS switch transistors in a way that both low-voltage and low-power operations are maintained [6]. The effect of mismatch among controlling transistors on the full enter-referred offset of the comparator is every other important issue. When figuring out the dimensions of controlling transistors (MC1 − MC2), critical issues ought to be taken into consideration. First, the effect of threshold voltage mismatch and modern thing mismatch of the controlling transistors at the comparator enter-referred offset voltage. 2nd, the impact of transistor sizing on parasitic capacitances of the fn/fp nodes, i.e., CL, fn(p), and therefore the delay of the comparator. Even as larger transistors are required for higher matching; however, the increased parasitic capacitances are put off bottlenecks.

V.SIMULATION RESULTS

In order to compare the proposed comparator with the conventional and double-tail dynamic comparators, all circuits have been simulated in a 90nm CMOS technology with VDD

= 1V. The comparators were optimized and the transistor dimensions were scaled to get an equal offset standard variation of σOS= 8 mV at the input common mode voltage of V cm = 1.1 V. Fig. 3 shows the layout of the comparator. Particular care was taken in the layout to avoid affecting delay and power of the comparator.

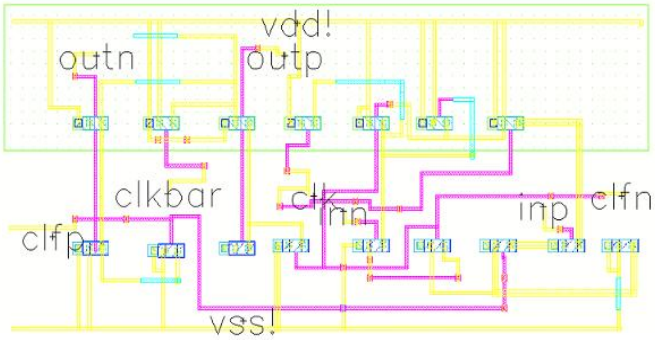


Figure.3. Layout schematic diagram of the proposed dynamic comparator.

Fig. 3(a) and (b) demonstrates the post-layout simulation results of the delay and the energy per conversion of the mentioned dynamic comparators versus supply voltage variation. As shown in Fig. 3(a), in comparison with the other two structures, the delay of the proposed double tail dynamic comparator is significantly reduced in low-voltage supplies. It is obvious that at high supply voltages, all structures have approximately similar performances, about 200 psclk to-output delay (including clock buffer) with 0.65 pJ/bit conversion for 8-mV offset. However, by decreasing the supply voltage, three structures start to behave differently. It is evident that the double-tail topology can operate faster and can be used in lower supply voltages, while consuming nearly the same power as the conventional dynamic comparator. The case is even much better for the proposed comparator when compared to the conventional double-tail topology. For instance, the proposed comparator can operate in 0.6 V supply at the cost of 106 fJ/conversion with 840 ps delay versus 1.81 ns for the conventional double-tail comparator and 3.5 ns for the conventional topology. Our simulations show that if the circuit is optimized for VDD = 0.6 V, the results would be even better for the proposed circuit [5].

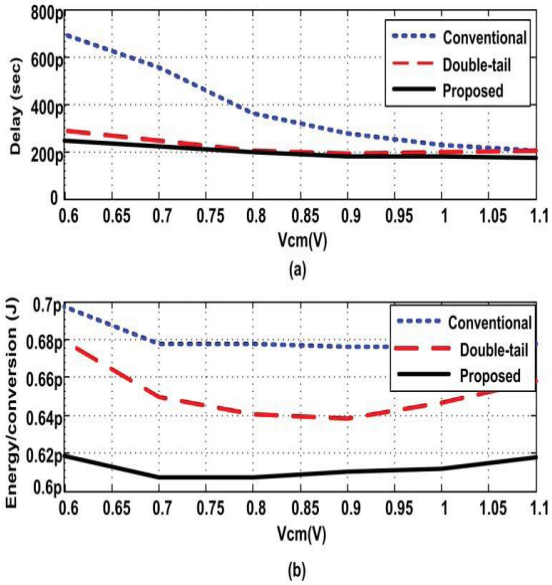


Figure.4. (a) Post-layout simulated delay and (b) energy per conversion as a function of input common-mode voltage

Fig. 4 shows the simulated performance as a function of input common-voltage (Vcm). Generally in the double-tail topologies, the delay of the comparator is less influenced by the variation of the input common-mode voltage in comparison with the conventional dynamic topology and thus has a wider common-mode range. The power consumption is nearly equal [3].

Table.1. Summary of the comparator performance

.	**Value**
Technology	90nm CMOS
Supply Voltage	1V
Average Power Dissipation (W)	234.3E-6
Delay (Sec)	340E-12
Energy Efficient (J)	0.34E-12
Area (nm^2)	26.8*13.1

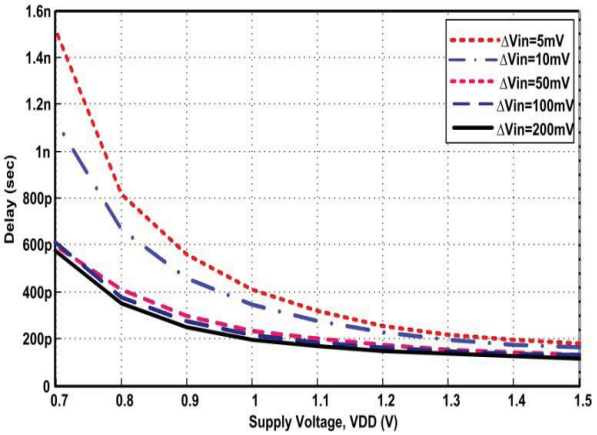


Figure.5. Delay of the proposed comparator versus supply voltage (VDD)

Fig. 5 depicts the dependence of the comparator delay on power supply level at various differential input voltages. For △Vin= 10 mV, the delay is 460 ps at VDD = 0.9 V. This delay drops from 460 to 162 ps when VDD changes from 0.9 to 1.5 V. In addition, at a given VDD, the larger the differential input voltage, the smaller the comparator delay will be.

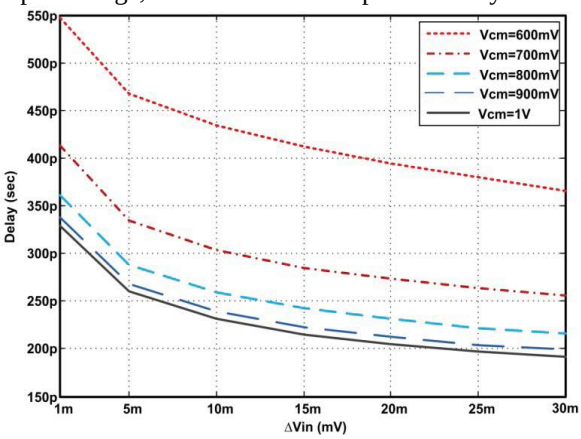


Figure.6. Delay of the proposed comparator versus input voltage difference

Fig. 6 shows the simulated delay of the comparator versus differential input voltage under different conditions of input common-mode voltage (Vcm) at VDD = 1 V. The delay of the comparator at △Vin= 1 mV and Vcm= 700 m is 413 ps. For a given value of Vcm, the delay decreases as differential input voltage increases. Furthermore, the delay is also dependent on the variation of common-mode voltage. For example, at △Vin= 10 mV, the delay increases by 64 ps, from 239 to 303 ps, as Vcm decreases from 900 to 700 mV.

VI.CONCLUSIONS

In Design of a Low-Voltage Double-Tail Comparator, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Based on theoretical analyses, a new dynamic comparator with low-voltage low power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 90nm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent.

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