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A Novel RCA Designed and Implemented for Reducing Delay Time and Power Consumption

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Abstract:
In this brief, the implementation of ripple carry architecture and RNS converters base on well-known regular and modular parallel prefix adders is analyzed. The Integrated design implementation marks shows a important delay reduction and area multiply with double the time improvements, all this at the cost of higher power consumption, it is the most important reason preventing the use of R.C Architecture to achieve high-speed reverse converters in nowadays systems. Hence, to solve the high power consumption problem, novel specific hybrid RCA (Ripple carry architecture) components that provide better trade-off between delay and power consumption are herein presented to design reverse converters. A methodology is also described to design reverse converters based on different kinds of prefix adders. This methodology helps the designer to adjust the performance of the reverse converter based on the target application and existing constraints.

Index terms: RCA, RNS Parallel prefix address

I. INTRODUCTION

In the world of battery-based and portable devices, the residue number system (RNS) can play a significant role due to its low power features and competitive delay. The RNS can provide carry free and fully parallel arithmetic operations for several applications, including digital signal processing and cryptography.

However, its real usage requires forward and reverse converters to be integrated in the existing digital systems. The reverse conversion, i.e., residue to binary conversion, is a hard and time-consuming operation. The RNS consists of two main components forward and the reverse converter that are integrated with the existing digital system.

The forward converter performs the operation of converting the binary number to the modulo number whereas the reverse converter performs the operation of reverse converting the modulo number to the binary number which is the hard and time consuming process compared with the forward converter.

In this brief, for the first time, we present a comprehensive methodology to wisely employ R.C Architecture in carefully selected positions in order to design fast reverse converters. The collected experimental results based on area, delay, and power consumption show that, as expected, the usage of the R.C Architecture to implement converters highly increases the speed at the expense of additional area and remarkable increase of power consumption.

The significant growing of power consumption makes the reverse converter not competitive. Two power-efficient and low-area hybrids R.C Architecture are presented in this brief to tackle with these performance limitations, leading to significant reduction of the power delay product (PDP) metric and considerable improvements in the area-time2 product (AT2) in comparison with the original converters without using parallel-prefix adders.

II. PARALLEL-PREFIX STRUCTURE:

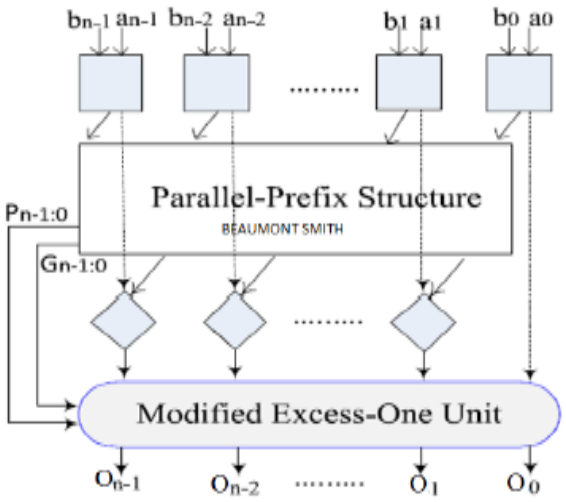


Figure.1. Parallel-prefix structure

Parallel-prefix adders with its high-speed feature have been used in the RNS modular arithmetic channels. This performance gain is due to parallel carry computation structures, which is based on different algorithms such as [15]–[17]. Each of these structures has distinct characteristics, such as Sklansky (SK), and Kogge–Stone (KS) as they have the maximum and minimum fan-out, respectively, both providing minimal logic depth. Minimum fan-out comes at the expense of more circuit area [18]. Therefore, hardware components selection should be undertaken carefully.

III. RIPPLE CARRY ARCHITECTURE:

Ripple-carry adders (RCA) this leads to significant speed degradation, due to the linear increase of the delay in the RCA

with the number of bits. Parallel-prefix adders can be used in the RNS reverse converters to bind the delay to logarithmic growth. However, in reverse converters, several parallel-prefix adders are usually required. Even when only one adder is used, the bit length of this adder is quite large. Consequently, this results in high power consumption notwithstanding its high speed. Therefore, in this section, two approaches that take advantage of the delay properties of the parallel prefix adders with competitive power consumption are introduced. Usually, one regular binary addition is required in reverse converter structures to achieve the final binary representation. This final addition has an important effect in the total delay of the converter due to the large bit-length of the operands. A thorough assessment of this final regular addition in recent converter designs shows that one of the operands has some constant bits with value 1 as highlighted by the following lemma, which applies to a class of converters described. The regular CPA with end around carry (EAC) is by default a moduli $2n - 1$ adder with double representation of zero, but in reverse converters a single representation of zero is required. So, a one-detector circuit has to be used to correct the result, which imposes an additional delay. However, there is a binary-to-excess-one converter (BEC) [20], which can be modified to fix the double-representation of zero issue. In Fig. 3. The HMPE consists of two parts: 1) a regular prefix adder and 2) a modified excess-one unit. First, two operands are added using the prefix adder, and the result is conditionally incremented afterward based on control signals generated by the prefix section so as to assure the single zero representation.

3.1 Conversion Architecture:

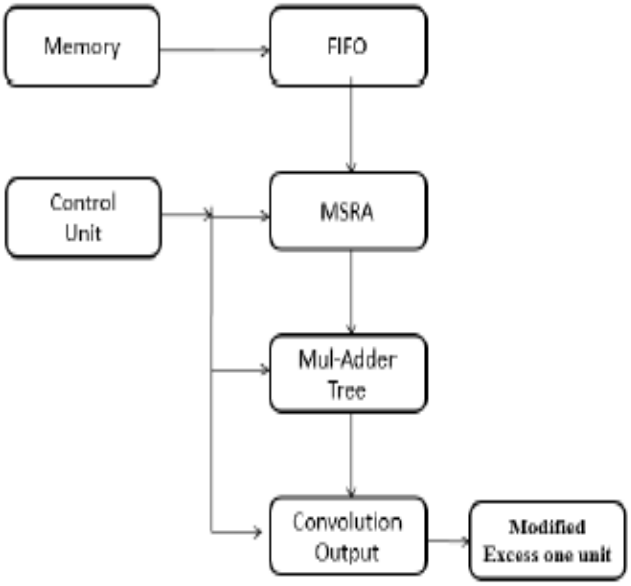


Figure.2. Conversion Architecture

If the existing architecture is working slowly for double representation zero operation, to eliminate the problem we use external unit. Fig.2. Shows the proposed system is used fully series and fully parallel operation. Proposed system components are:

1. MSRA

2. Multiplicand and Ripple carry adder tree

3. Control unit

4. Convolution process

5. Modified excess one unit

3.2. Multiplicand and Ripple carry adder tree

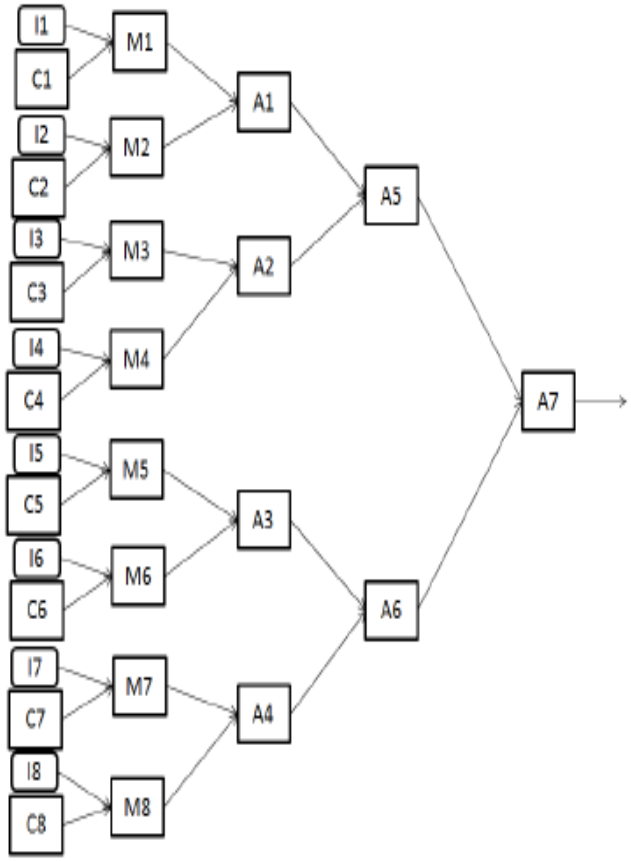


Figure.3. Multiplicand and Ripple carry adder tree

The MSRA is an implemented registers array having each register with 8 bit wide, to be able to store a pixel. The MSRA is designed to perform left/right shifting. Moreover, it allows for the up/down shifting along the vertical direction. The output signals of each registry are connected to the Mul-Adder Tree to perform the signed to perform the left/right shifting products with the weights of the kernel matrix. The output unit includes an output buffer to store 4 pixels, and a data normalization unit. The normalization unit is required to normalize the size of the convolved pixel to 8 bits. The Control Unit coordinates the data stream within the system architecture. Mainly, it drives the control signals needed to shift the MSRA and to acquire a new row/column.

3.3 Control Unit

The output unit includes an output buffer to store 4 pixels, and a data normalization unit. The normalization unit is required to normalize the size of the convolved pixel to 8 bits. The Control Unit coordinates the data stream within the system architecture. Mainly, it drives the control signals needed to shift the MSRA and to acquire a new row/column.

3.4 Convolution

Convolution is a mathematical way of combining two signals to form a third signal. It is the single most important technique in Digital Signal Processing. Using the strategy of impulse decomposition, systems are described by a signal called the impulse response. Convolution is important because it relates the three signals of interest: the input signal, the output signal, and the impulse response

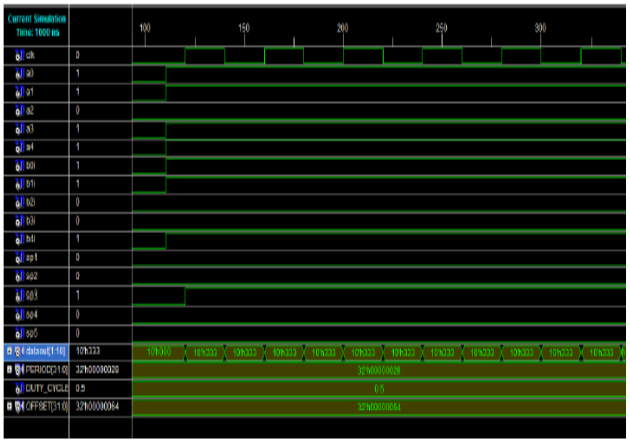
IV. SIMULATION RESULT

Simulation

The simulation of reverse converter units are synthesized with the device xc2s50-6, package of tq144 and corresponding Timing waveforms are taken from the Test Bench as shown in The designed reverse converter is synthesized using Xilinx project navigator for device xc2s50-6tq144 the resource utilization.

Table 1. Resource utilization

Device Utilization Summary (Estimated Values)			
Logic Utilization	Used	Available	% Utilization
Number of occupied slices	8	768	1%
Number of 4input LUT's	14	1,536	1%
Number of slices	8	8	100%
containing only related logic			
Number of bonded IOB's	24	92	26%
Total equivalent gate count for design	84	--	--

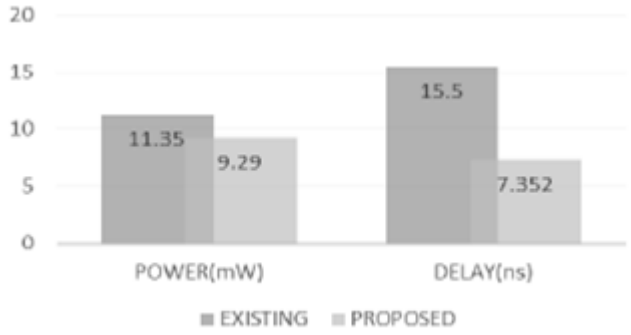


Synthesize Result

Table.2. shows the synthesize result for using Xilinx project navigator for device xc2s50-6tq144

Table 2. Synthesize result

	EXISTING	PROPOSED
POWER(mW)	11.35	9.29
DELAY(ns)	15.50	7.352



V. CONCLUSION

This brief presents a method that can be applied to most of the current reverse converter architectures to enhance their performance and adjust the cost/performance to the application specifications. Furthermore, in order to provide the required trade-offs between performance and cost, new RCA design and parallel distributed arithmetic convolution technique components are introduced. These components are specially designed for reverse ripple carry adders. Implementation results show that the RCA based on the suggested components considerably improve the speed when compared with the original converters, which do not use any adder, and reduce the power consumption compared with the converters that exclusively adopt adders

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