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Efficient Implementation of Discrete Orthogonal Transforms for Real Valued Data using A Serial - Parallel Vector Matrix Multiplier

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Abstract:
In this paper we have proposed a multiplier less 2-D systolic architecture for efficient implementation of discrete orthogonal transforms for real valued data using a serial-parallel vector matrix multiplication scheme. The proposed structure is highly regular, simple and yields high throughput due to massive parallelism across the 2-D architecture. The structure yields high throughout since the duration of each time-step is reduced considerably over existing word level structures. The area and time complexities of the proposed structure are 0 (N^2) and 0 (N ($n+\log_2 n$)) respectively.

Keywords: Algorithm, Discrete Orthogonal Transforms, VLSI

Introduction

Discrete orthogonal transforms have evolved quite rapidly over the last three decades for their speech and image processing applications. The discrete Fourier transform (DFT) is most popular and one the oldest among these orthogonal transforms. Following the fast Fourier transform (FFT) of Cooley and Tukey [1]. Several algorithms have, therefore, been developed for fast computation of the DFT [2]. The discrete Hartley transform (DFT) [3] has become popular in recent years, as a real valued alternative to the DFT for several one- and two-dimensional signal-processing applications for avoiding complex arithmetic operations. Hence many a fast algorithms has been reported in the literature [3,4] for efficient computation of DHT. Amongst all orthogonal transforms, the discrete cosine transform (DCT) [5] is the. most efficient for the compression of speech and image data [6]. Performance of DCT is shown to be comparable to the optimal Karhunen Loeve Transform (KIT) [5,7] for the purpose of data compression, feature extraction, and filtering applications. Therefore, several fast algorithm have been developed for efficient computation of the DCT, in general purpose computers [8,9]. In systolic architectures, the desired data are pumped rhythmically in a regular interval across the PEs for yielding high throughput by fully pipelined processing. Keeping these facts in view, some systolic architectures have been suggested for the VLSI implementation of the DFT, DCT and the DHT. To achieve saving in hardware and to have throughput of computation, prime-factor decomposition scheme have been employed for VLSI implementation of discrete orthogonal transforms. Jones [2] has proposed a novel systolic implementation of the row—column method for prime-factor DFT. Owens and Ja' Ja' [10] have, suggested a prime factor architecture for DFT basing on so called small n algorithm and several other iterative methods. Chakrabarti and Ja' Ja' [12] have suggested a systolic architecture for prime-factor DHT that is computed via four temporary outputs. Cho and Lee [11] have suggested a straightforward ward implementation of prime-factor DCT. Lee and Huang [9] have proposed two systolic array architectures for prime-factor DCT that comprises of' two matrix multiplication units and a transposition unit. However, Prime-factor approach always involves significant hardware and time in the input and output interfaces for index mapping and storing of data matrices. Apart from that, structures for implementation of prime—factor algorithms require additional time as well as hardware for transposition of immediate result. In most practical situations, the input data is real valued. However, adequate emphasis has been given for efficient implementation of discrete orthogonal transforms in dedicated VLSI for real valued data Gou et al [13] have suggested a CORDIC based architecture for M-D DHT using a kind of 1 -D transform different from 1-D DHT. This architecture may. however, be used for implementation of 1-D prime-factor DHT adopting an appropriate mapping scheme [4] for converting 1-D input into its 2-D form.

In this paper we have suggested a multiplierless 2-D systolic array for efficient implementation of discrete orthogonal transforms using serial-parallel vector matrix multiplication scheme. The proposed structure is highly regular, simple and yields high throughput due to massive parallelism across the 2-D architecture. It provides significant saving in hardware and time over existing structures.The algorithm for bit serial implementation of discrete orthogonal transforms is given in Section 2. Section 3 deals with the proposed systolic architecture for implementation of discrete orthogonal transform. Hardware requirement and throughput rate of the proposed structure are discussed with time conclusion in Section 4.

2. Algorithm for Bit Serial Implementation of Discrete Orthogonal Transform

Let $X = [x_0, x_1, x_2 \ldots\ldots, x_{N-1}]^t$ be a data column vector and C be an N x N kernel matrix of an N-point orthogonal transform. The transformed vector of X is given by

$Y=CX=[y_0, y_1,\ldots\ldots y_{N-1}]^t$ (1)

The element of mth row of Y is given by

$$Y_m = \sum_{k=0}^{N-1} C_{mk} X_k \quad (2)$$

Let the element of the data column vector X be represented by the 2's complement code as follows:

$$X_k = -X_k^{n-1} 2^{n-1} + \sum_{j=0}^{n-2} X_k^j 2^j \quad (3)$$

where X_k^j is the jth bit of X_k which has a value of 0 or 1. n is the number of bits X_k carries X_k^{n-1} is the sign bit.

Substituting (3) into (2), we have

$$y_m = -\sum_{k=0}^{N-1} C_{mk} X_k^{n-1} 2^{n-1} + \sum_{k=0}^{N-1} \sum_{j=0}^{N-2} C_{mk} X_k^j 2^j \quad (4)$$

Each Y_m for m =0, 1, ….. N-1 given by (4) may be implemented in a systolic array so that N-point output of an orthogonal transform may be computed from a 2-D systolic architecture comprised of N systolic arrays described in the following section.

3. Systolic Architecture For Serial — Parallel implementation of implementation of Discrete Orthogonal Transform

The proposed architecture for serial parallel implementation of N-point discrete Orthogonal transform is shown in Fig. 1. When the maximum input data size is taken to be of n bits, extra $\log_2 n$ bits are taken as guard bits for internal arithmetic of the PEs and the accumulators with a view to prevent overflow. Therefore, $\log_2 n$ number of zeroes are inserted before the MSB of each input word and the adders in each PE and accumulator are designed to perform $(n+\log_2 n)$ -bit additions. The input data sequence $x_0, x_1, x_2 . \ldots\ldots, x_{N-1}$ is shifted sequentially in time into N-stage Q shift registers at data rate 1/T. The contents of Q shift registers are bit-parallely loaded into the R shift registers, staggered by one time-step with respect to its preceding one.
The data in R shift registers is then bit —serially shifted out with least significant bit first. N x N identical processing elements (PEs) are arranged in N rows and N columns The function of each PE is shown in Fig 2. Detail structure of a processing element is shown in Fig.3. After N time—steps. the first output bit arrives in the accumulator A_0. Then the subsequent bits arrive in the accumulators in the subsequent time-steps. In each accumulator, the subsequent data are added to its earlier content with a hard wire I-bit right shift shown in Fig.4. The same operations are repeated $(n+\log_2 n)$ times except for the last time (sign bit) when a subtraction instead of addition is performed.

FIG.1: 2-D SYSTOLIC ARCHITECTURE FOR IMPLEMENTATION OF THE DISCRETE COSINE TRANSFORM

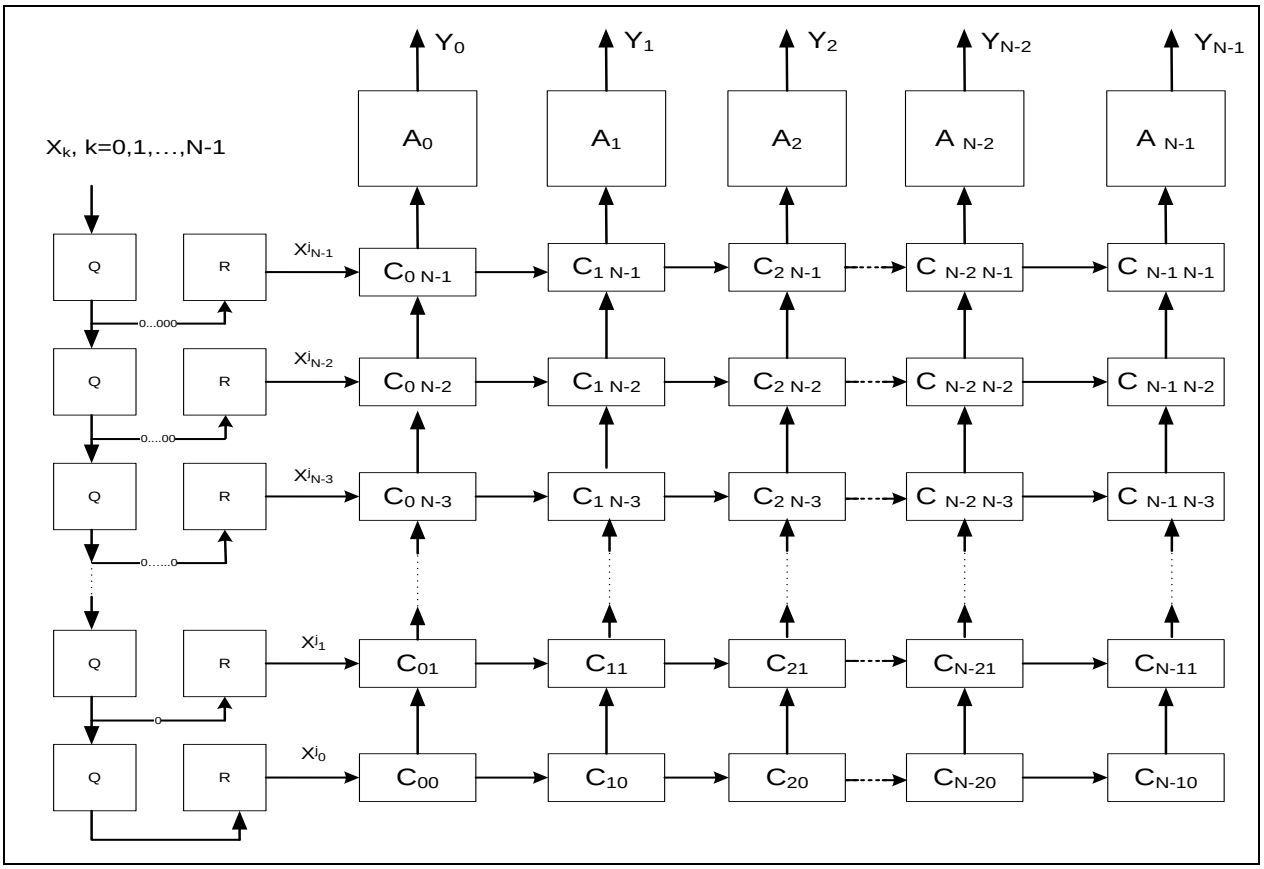


FIG. 2 (A) FUNCTION OF EACH PROCESSING ELEMENT

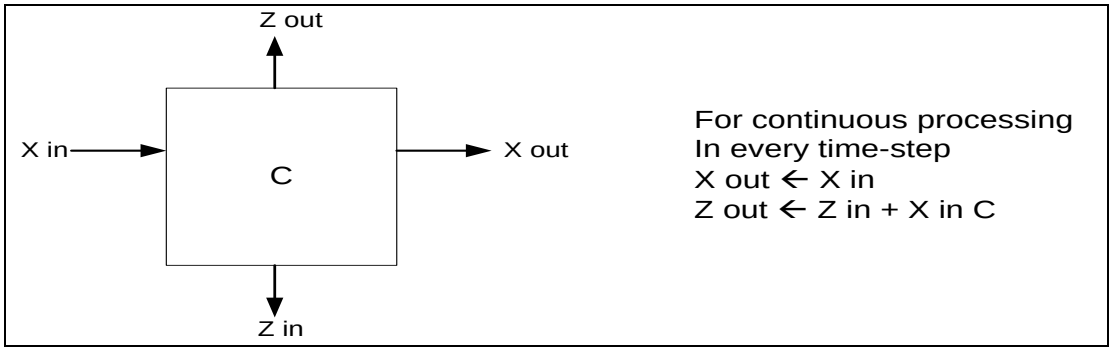


FIG. 2 (B) ACCUMULATOR

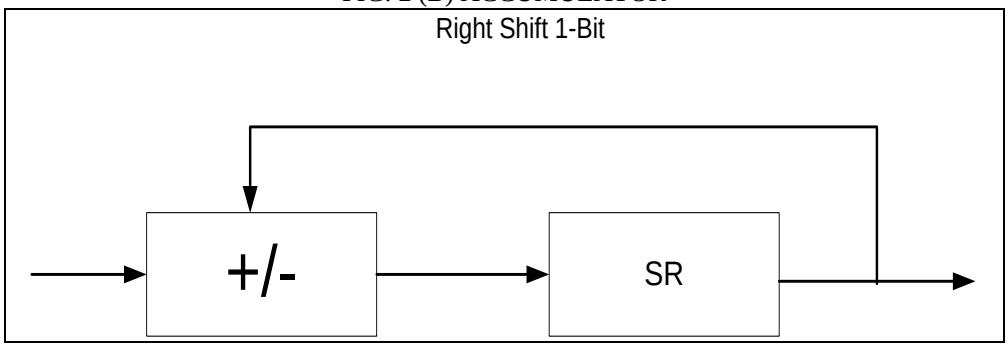
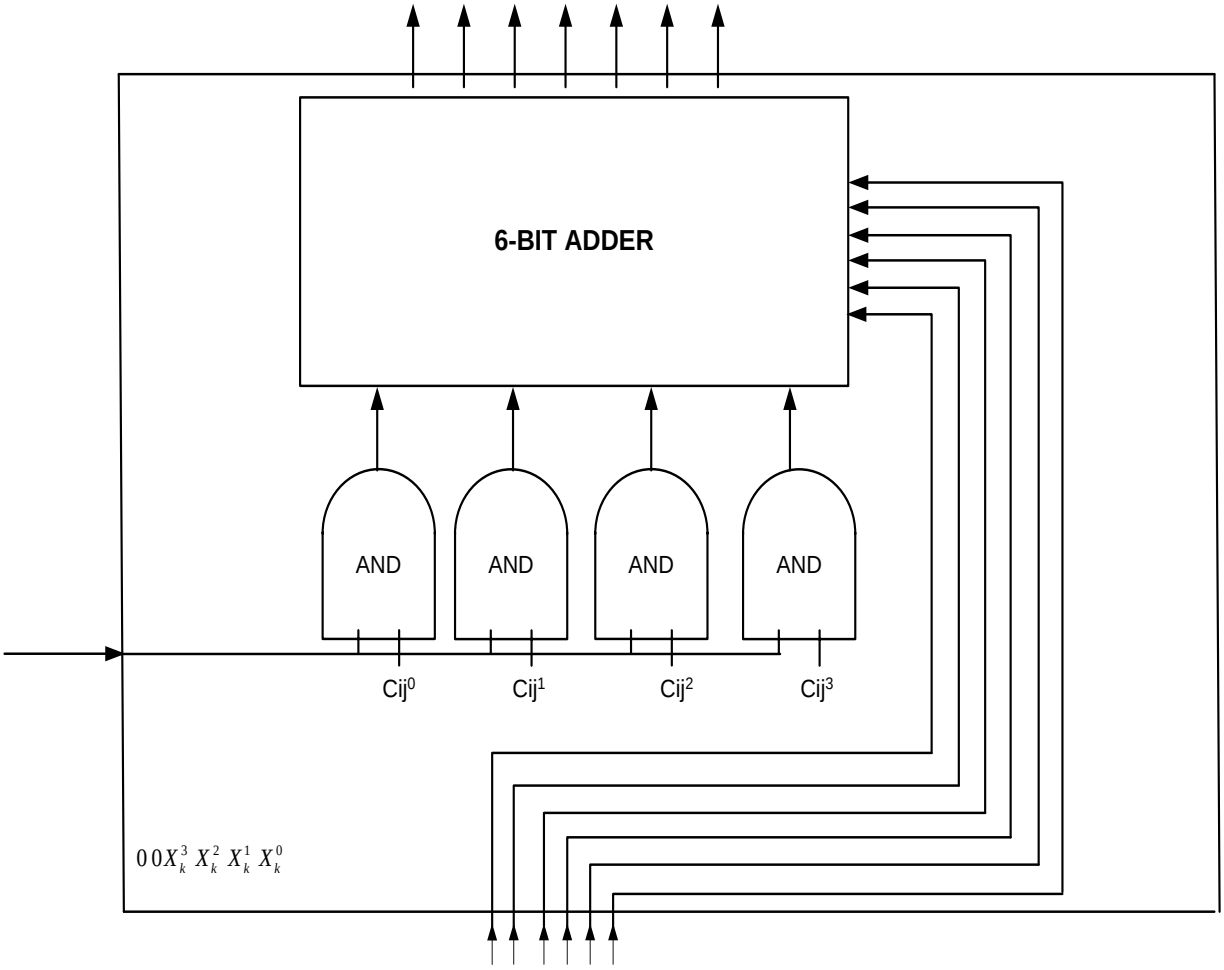


FIG.3: DETAILED STRUCTURE OF A PROCESSING ELEMENT (FOR WORD LENGTH N=4)



4. Conclusion:

The proposed systolic architecture requires N x N number of identical PEs arranged in N rows and N columns where each PE performs an addition of $(n+\log_2 n)$- bit words during each time-step. Each PE consists of n AND gates and one adder for addition of two $(n+\log_2 n)$- bit words. The duration of each time-step, T, is therefore, same as the addition time of $(n+\log_2 n)$ bit words neglecting one gate delay for AND operation and latching time). The first transformed component is obtained after $(N+n+\log_2 n)$ time-steps from the accumulator A_0 The successive transformed components are- obtained in each subsequent time-steps. The first set of transformed output is obtained after $(2N+n+\log_2 n-1)$ time-steps. However successive sets of discrete orthogonal transforms may be obtained in every $(n+\log_2 n)$ time-steps. The throughput rate of this structure is $N/(n+\log_2 n)T$. The area and time complexities of the proposed structure are $O(N^2)$ and $O(N(n+\log_2 n))$ respectively. The VLSI performance measure of the proposed structure $O(N^4 (n+\log_2 n)^2)$. Multiplication is avoided in the serial-parallel scheme for which it has been possible to avoid multipliers to have consequent saving in hardware. Besides, one addition of two $(n+\log_2 n)$- bit words is performed in each time-step. So the duration of each time-step is considerably reduced over existing word level structures. The reduction in the duration of time-step and massive parallelism employed in the structure results high throughput rate. The proposed structure, will be highly useful for real—time implementation of discrete orthogonal transforms.

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