



# Simulation and Analysis of Various Switching Fault of Five Level Neutral Point Clamped Inverter Fed Induction Motor Drive

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## Abstract:

This paper present the simulation of three phase five level neutral point clamped (NPC) inverter fed induction motor drive and the simulation is done by MATLA/SIMULINK. It has been widely applied in power conversion at high and medium voltages. The sinusoidal pulse width modulation (SPWM) control strategy method is used for neutral point clamped inverter to reduce the total harmonic distortion in the output waveform. The various switching fault are analyzed and effect of faulty switches on the performance of five level NPC fed induction motor has been studied.

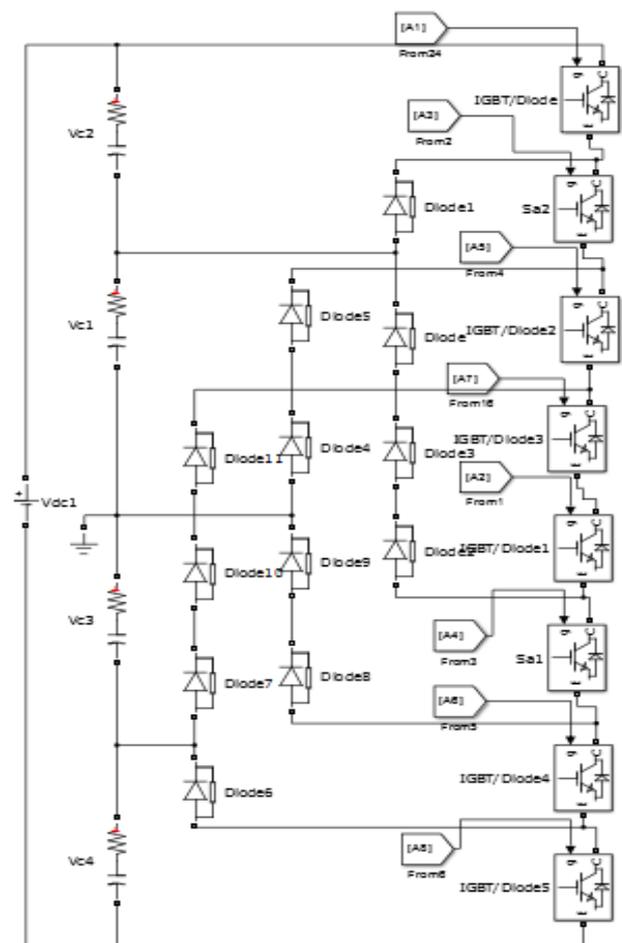
**Keywords:** NPC, Sinusoidal PWM, IGBT open, IGBT short, GATE open, GATE short, Switching State, Five Level Inverter.

## I. INTRODUCTION

Nowadays, three phase induction motor is widely used because of its reliable operation, simple construction and lightness. For motor control AC induction motor drive is the fastest growing sector of the motor control. Due to improvement in power electronics technology, in the last three decade DC motor are progressively replaced by a AC motor[1][2]. DC motors have disadvantage of higher maintenance, higher rotor inertia and cost problem with brushes and commutator.

The AC machines do not have the disadvantages of DC machine. The variable speed drive commonly used in industry[3]. Multilevel inverter (MLI) are well proven as a standard configuration for the pulse width modulation (PWM) inverter drives due to utility of high dynamic response, fast power switching semiconductor devices and good spectral performance. The high frequency pulse width modulation (PWM) techniques used to improve output waveform in multilevel inverter. There are many types of PWM techniques like Sinusoidal pulse width modulation technique (SPWM), Single PWM technique, Multiple PWM technique, Space vector pulse width modulation technique (SVPWM), Selective harmonic elimination pulse width modulation techniques (SHE-PWM). Out of that selective harmonic elimination space vector modulation and sinusoidal PWM techniques are generally used[4]. Multilevel inverter MLI to obtain better quality output voltages with lower dv/dt and excessively lower distortion. They can operate with a lower power switching frequency and also reduced voltage stress is offered on power switching device[8]. The possible faults in NPC inverter fed induction motor drives such as switch open, switch short, diode open and diode short fault. Fault in control equipment like gate open and gate short fault[5][6].

inverter. The neutral point clamped inverter obtains the staircase output waveform voltage. If  $m$  is the no. of level than no of capacitor required on the DC bus are  $(m-1)$ , the no. of power electronic switches per phase are  $2(m-1)$  and no. of diode per phase are  $4(m-2)$ . The DC voltage has three level using two capacitor  $C1$  &  $C2$ , for five level using four capacitor[4][7][8]



**Figure.1. Diode-Clamped Five Level Inverter Circuit Topology**

## II. PROPOSED NPC TOPOLOGIES

The multilevel inverter broadly classified are diode clamped MLI, flying capacitors MLI, cascade H-bridge MLI. The diode clamped multilevel inverter, also called neutral point clamped

**Table.1. Five Level Switching State**

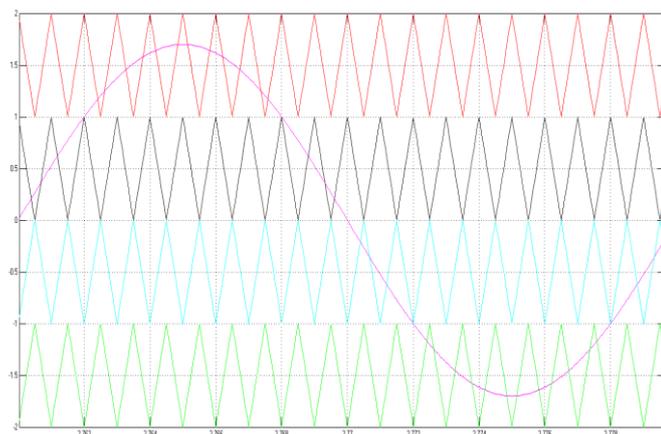
TERMINAL VOLTAGE SWITCHING STATE								
	SA1	SA2	SA3	SA4	SA5	SA6	SA7	SA8
2VDC	1	1	1	1	0	0	0	0
VDC	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-VDC	0	0	0	1	1	1	1	0
-2VDC	0	0	0	0	1	1	1	1

**III. METHODOLOGY**

In sinusoidal pulse width modulation (SPWM), the sinusoidal wave or reference signal compared with carrier signal and the width of each signal is varied in proportional to the sine wave at the same pulse. SPWM maintaining the width of all pulses same as in the case of multiple PWM.

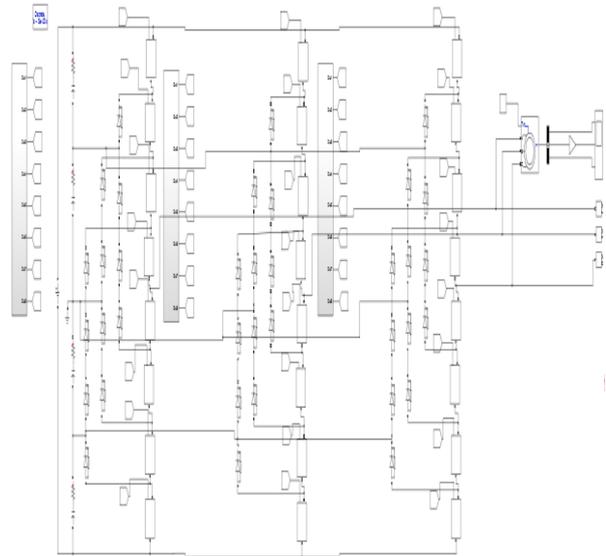
Triangular wave or carrier signal has present Amplitude parameter, frequency parameter, phase of each carrier and offset between the each carrier. The Reference wave also present freedom in following parameter Frequency, amplitude, phase angle and injection of zero sequence signal. Carrier based modulation technique are categorized as: Level shifted pulse width modulation (LS-PWM), Phase shifted pulse width modulation (PS-PWM) and Hybrid (H).

The proposed phase opposition disposition scheme carrier are all in phase below and above in zero reference[9]. A 180 degrees of phase shift between those above and below in zero reference. Carrier and reference waveform of five level POD scheme are shown in fig. 2. During comparison in this method, when the reference wave is smaller than carrier signal, output is '0' and when the value of the reference wave is greater than the carrier signal, output is '+1'. Similarly the '-ve' half cycle, when the reference wave is greater than the carrier wave, output is '-1' and whereas when the value of reference wave is smaller than the carrier wave, output becomes '0'. This switching signals to be provided to different switches of the above mentioned NPC topology[1].

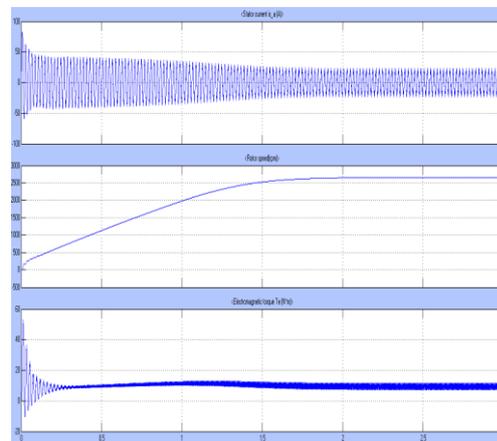


**Figure.2. Phase Opposition Disposition**

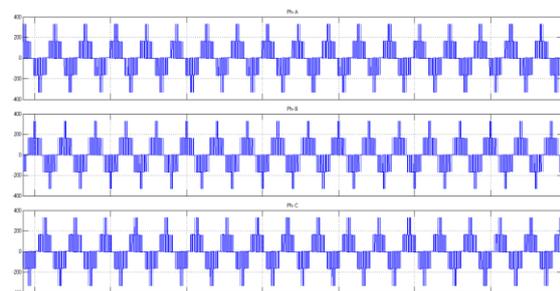
**IV. MATLAB/SIMULINK ANALYSIS**



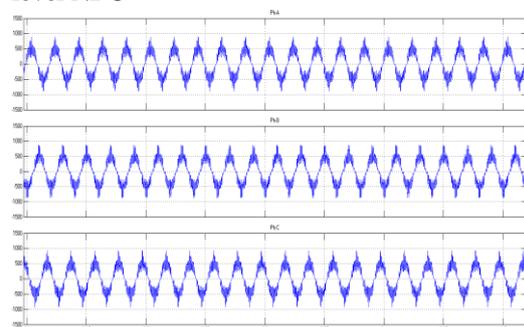
**Figure.3. Simulation Model of Five Level NPC Fed Induction Motor Drive**



**Figure.4. Performance Characteristics of Stator Current, Speed and Torque**



**Figure.5. Simulated Waveform of Output Line voltage of 5-level NPC**



**Figure.6. Line to Line Voltage of Five Level NPC Inverter**

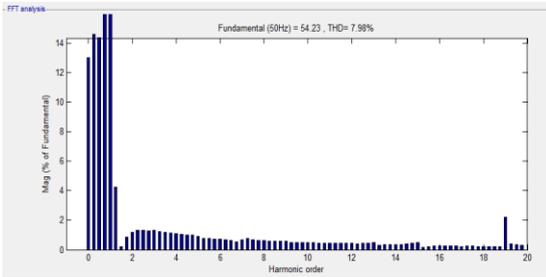


Figure.7. THD Analysis of Stator Current

## V. FAULT ANALYSIS

### CASE 1: IGBT OPEN FAULT

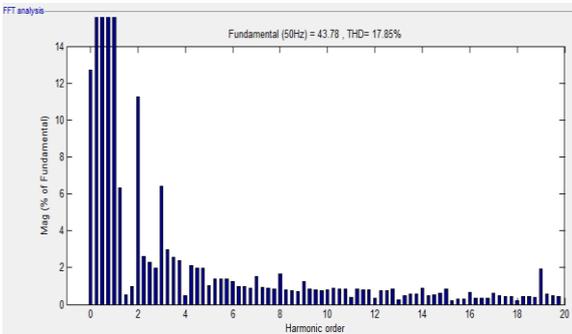


Figure.8. THD Analysis of Stator Current after IGBT Open Fault.

### CASE 2: IGBT SHORT FAULT

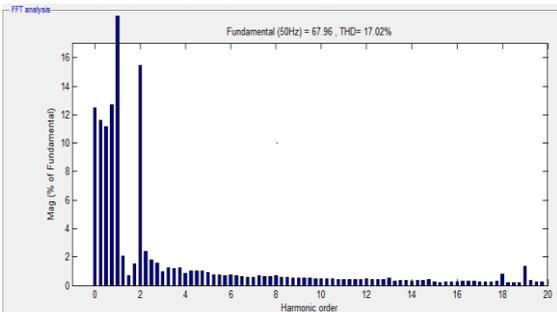


Figure.9. THD Analysis of Stator Current after IGBT Short Fault

### CASE 3: GATE OPEN FAULT

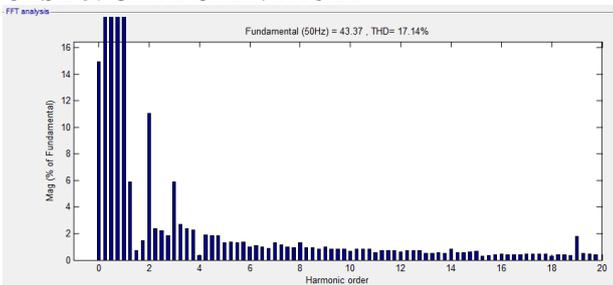


Figure.10. THD Analysis of Stator Current after GATE Open Fault

### CASE 4: GATE SHORT FAULT

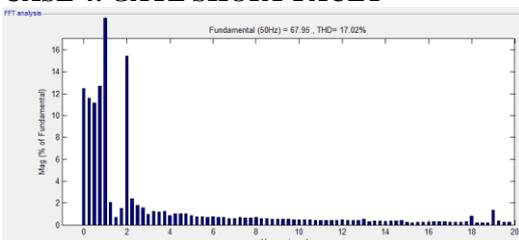


Figure.11. THD Analysis of Stator Current after GATE Short Fault

Comparison table of THD analysis as shown in below:

Table.2. Total Harmonic Distortion Of Stator Current Before And During Igbt Short/Open Fault

Stator current THD before IGBT fault	Stator current THD after IGBT open fault	Stator current THD after IGBT short fault
7.98	17.85	17.02

Table.3. Total Harmonic Distortion Of Stator Current Before And During Gate Short/Open Fault

Stator current THD before GATE fault	Stator current THD after GATE open fault	Stator current THD after GATE short fault
7.98	17.14	17.02

## VI.CONCLUSION

This paper has been addressed a different analysis for fault in (IGBT/DIODE) of five level neutral point clamped inverter fed induction motor drive. The performance of the three phase five level NPC inverter has been explained and it can be observed that switching fault and gate fault degrades the performance of the drives. Study of various PWM switching techniques. Waveform of torque, speed of the motor drive and stator current has been studied. The modeling of three phase five level inverter feeding induction motor drive was done and simulated using MATLAB/SIMULINK environment. Study total harmonic distortion THD reduced as the level of inverter is increase.

## VII. REFERANCE

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