ISSN XXXX XXXX © 2016 IJESC

Research Article Volume 6 Issue No. 12

Design and Implementation of CMOS ALU using Reversible Logic

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Abstract:
Reversible logic gates have received great attention in the recent years due to its ability to reduce power dissipation which is the main requirement in low power digital design. It has wide applications in advance computing, low power CMOS design, optical information processing, DNA computing, bio information, quantum computation and NANO technology. Conventional digital circuits dissipate a significant amount of energy because the bits of information are erased during the logic operations. Thus if logic gates are designed such that the information bits are destroyed. The power consumption can be reduced dramatically. The information bits are not lost in the case of reversible computation. This has led to the development of reversible gates. ALU is a fundamental building block of central processing unit (CPU) in any computing systems; the reversible arithmetic unit has high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder. Various arithmetic operations can be realized. In this work ALU based on a reversible low power control unit for arithmetic and logic operations is proposed. In our design, the full adder are realized using synthesizable; low quantum cost, low garbage output peres gate. This work presents a novel design of arithmetic and logic using reversible control unit. This reversible ALU has been designed and verified using S-EDIT, W-EDIT in TANNER tool with the help of CMOS 0.125µm technology.

Keywords: Reversible logic, ALU, Power optimization

I. INTRODUCTION

A processor is a main part of any digital system. And an ALU is one of the main components of a microprocessor. To give a simple analogy, CPU works as a brain to any system and ALU works as a brain to CPU. So it's a brain of computer's brain. They are consists of fast dynamic logic circuits and have carefully optimized structures. Of total power consumption in any processor, CPU accounts a significant portion of it. ALU also contribute to one of the highest power density locations on the processor, as it is clocked at the highest speed and is busy mostly all the time which results in thermal hotspots and sharp temperature gradients within the execution core. Therefore, these motivate us strongly for a energy efficient ALU designs that satisfy the high performance requirements, while reducing peak and average power dissipation. Basically ALU is a combinational circuit that performs arithmetic and logical operations on a pair of n bit operands. Dynamic power is power consumed while the inputs are active. When inputs have AC activity, capacitances are charging and discharging and the power increases as a result. The dynamic power includes both the ac component as well as static component.

2.1Reversible Gates:

Several reversible gates have been proposed over the years, e.g., the Toffoli gate, the Fredkin gate etc. A 3-input and 3- output reversible logic gate was proposed input. It has inputs a, b, c and outputs x, y and z as shown in Fig 2.1

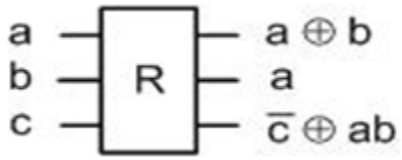

Figure. 1. ***Reversible logic gate***

2.1.1. Feynman Gate:

Feynman gate is a universal gate which is used for signal copying purposes or to obtain the complement of the input signal. The block diagram of Feynman gate is shown in fig. 2.1.1

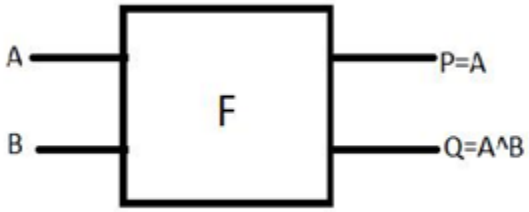

Figure.2. F*eynman Gate*

2.1.2. Fredkin Gate:

It is a basic reversible 3- bit gate used for swapping last two bits depending on the control bit. The control bit here is A, depending on the value of A, bits B and C are selected at outputs Q and R. When A=0, (Q=B, R=C) whereas when A=1, (Q=C, R=B). Its block diagram is as shown in fig. 2.1.2

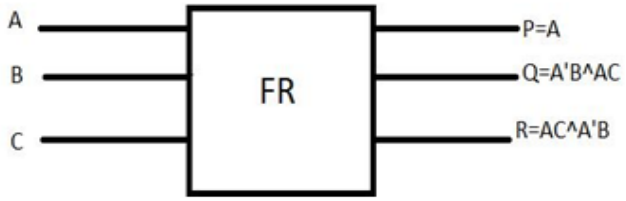

Figure. 3.*Fredkin Gate*

2.1.3. Peres Gate:

It is a basic reversible gate which has 3- inputs and 3-outputs having inputs (A, B, C) and the mapped outputs (P=A, Q=A^B, R= (A.B) ^C). The block diagram is as shown in fig.2.1.3

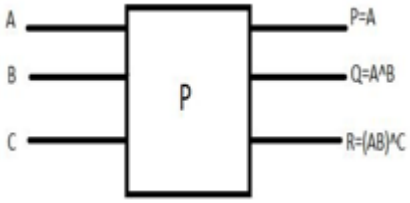

Figure. 4. *Peres Gate*

2.1.4. Toffoli Gate:

Toffoli gate is a universal reversible gate which has three inputs (A, B, C) mapped tothree outputs (P=A, Q=B, R= (A.B) ^C). The block diagram of Toffoli gate is shown in fig.2.1.4

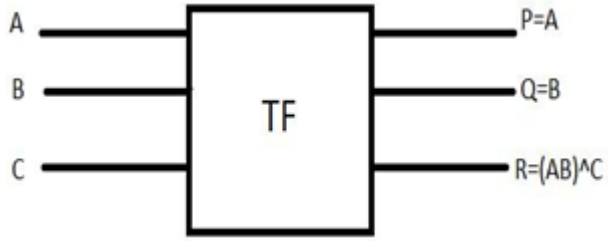

Figure.5.*Toffoligate*

2.1.5. TSG Gate:

TSG gate is a reversible gate which has four inputs (A, B, C, D) mapped to four outputs (P=A, Q=A^B, R=A^B^D, S=(A^B) ^D^AB^C). The block diagram of TSG Gate is shown in fig.2.1.5

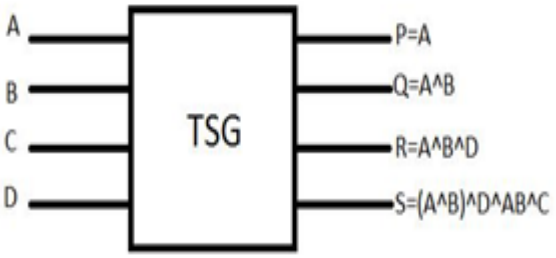

Figure.6.*TSG gate*

II.EXITING METHOD

In Central Processing Unit (CPU) of a computer, Arithmetic and Logic Unit (ALU) is a fundamental building block and even the simplest microprocessors contain ALU. It is responsible for performing arithmetic as well as logical operations such as addition, subtraction, increment, decrement, logical AND, logical OR, logical XOR and logical XNOR. The block diagram of ALU is shown in the figure 3.1. The schematic view of reversible ALU is shown in the figure 3.2

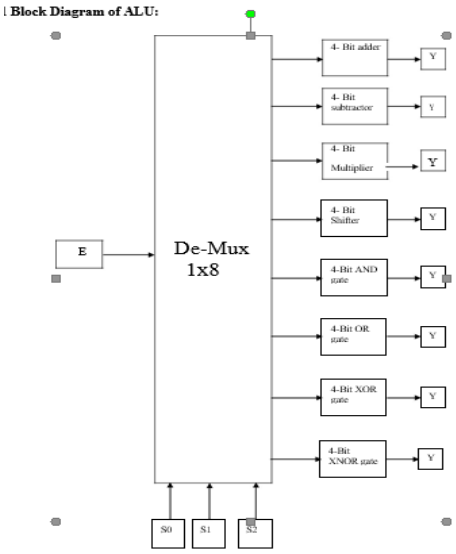

Figure.7. black diagarm of ALU

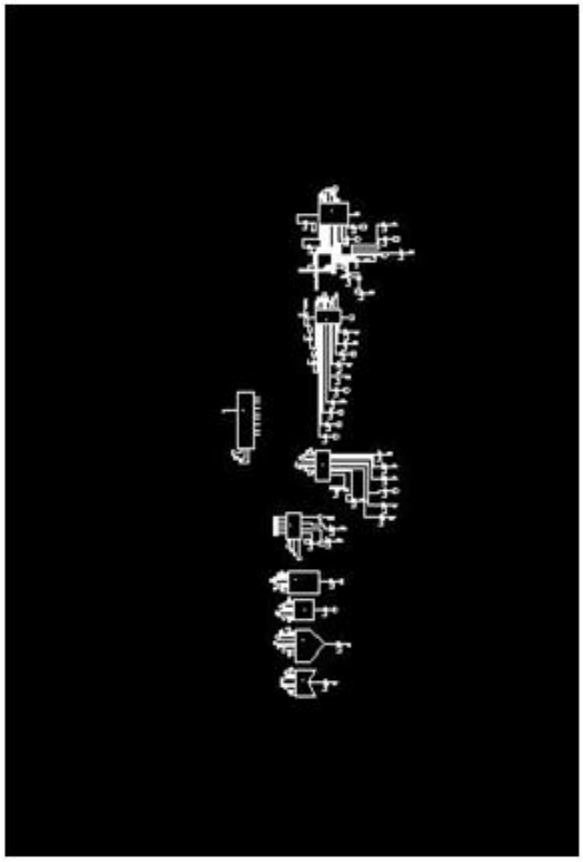

Figure.8. Schematic view of reversible ALU

III.PROPOSED WORK

6T Reversible Logic ALU:

There are two major, closely related, types of reversibility that are of particular interest for this purpose: physical reversibility and logical reversibility. To implement reversible computation, estimate its cost, and to judge its limits, it is formalized in terms of gate-level circuits. For example, the inverter (logic gate) (NOT) gate is reversible because it can be *undone*. The exclusive or (XOR) gate is irreversible because its two inputs cannot be unambiguously reconstructed from its single output. However, a reversible version of the XOR gate—the controlled NOT gate (CNOT)—can be defined by preserving one of the inputs. The three-input variant of the CNOT gate is called the Toffoligate. It preserves two of its inputs a,b and replaces the third c by c XOR(a.b) withC=0.This givesthe AND function and with a.b =1 this gives NOT function. Thus the Toffoli gate is universal and can implement any reversible Boolean function (given enough zero-initialized ancillary bits). More generally, reversible gates have the same number of inputs and outputs. A reversible circuit connects reversible gates without fan outstand loops. Therefore, such circuits contain equal numbers of input and output wires, each going throughan entire circuit. Similarly, in the Turing machine model of computation, a reversible Turing machine is one whose transition function is invertible, so that each machine state has at most one predecessor. A process is said to be physically reversible if it results in no increase in physical entropy; it is entropic. These circuits are also referred to as change recovery logic, adiabatic circuits or adiabatic computing. Although in practice non stationary physical process can be exactly physically reversible or isentropic, there is no known limit to the closeness with which we can approach perfect reversibility, in systems that are sufficiently well-isolated from interactions with unknown external environments, when the laws of physics describing the system's evolution are precisely known. Probably the largest motivation for the study of technologies aimed at actually implementing reversible computing is that they offer what is predicted to be the only potential way to improve the energy efficiency of computers beyond the fundamental vonNeumann-Landauer's limit of kT ln(2) energy dissipated per irreversible bit operation. The proposed 6T adder sum is generated using 2T XOR module twice, and carry is generated using NMOS and PMOS pass transistor logic devices.

The equations for 6T full adder design are:

SUM=(a xor b) cbar+ (a xor b)bar **c**

CARRY=(a xor b)bar a + (a xor b)c

In this design (a xor b) signal is passed to the pass transistor multiplexer made of two transistors to choose one among two. To generate carry (a xor b) is sent to multiplexer to choose between a, c. and to generate sum (a xor a) is sent to choose between c`, c.6T adder is shown in the below fig.

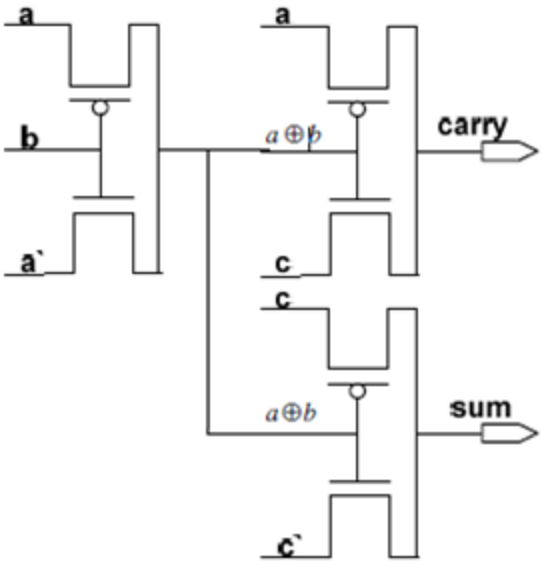

Figure.9. 6T adder

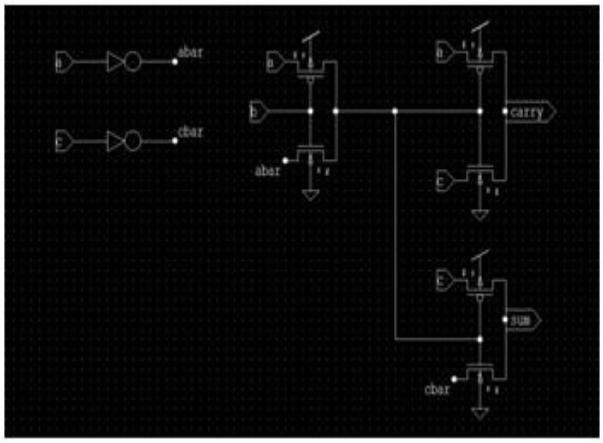

Figure.10.Schematic view of 6T adder

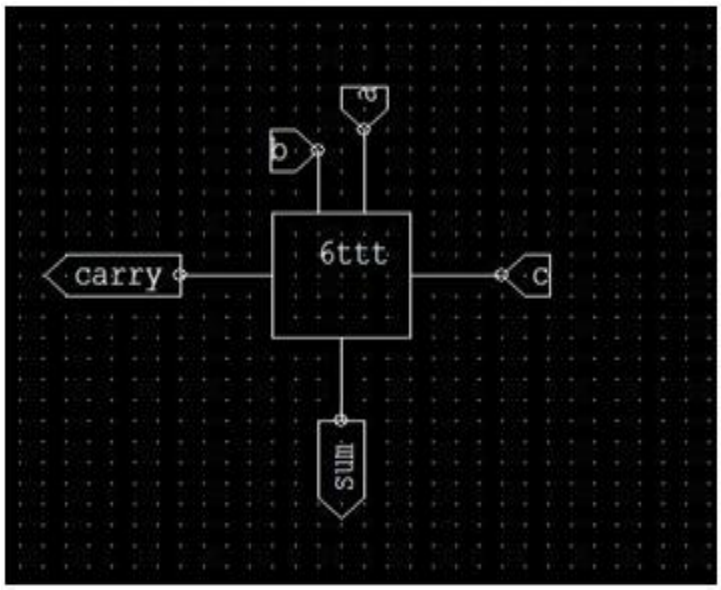

Figure.11.Symbolic view of 6T adder

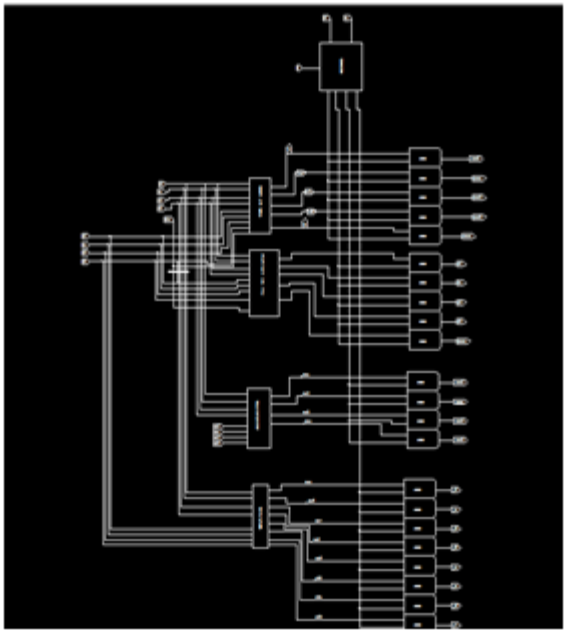

Figure.12.Schematic view of 6T Reversible ALU

IV.SIMULATION RESULTS

This section describes the performance of the proposed design using Tanner EDA tool on CMOS 0.18µm technology. The power analysis and no. of transistors used for 3 processors are clearly listed in the below table. The simulation results for 6T adder ALU is shown in the fig 5.1 and the bar graph representation for power and transistors used are shown in the fig 5.2 & 5.3

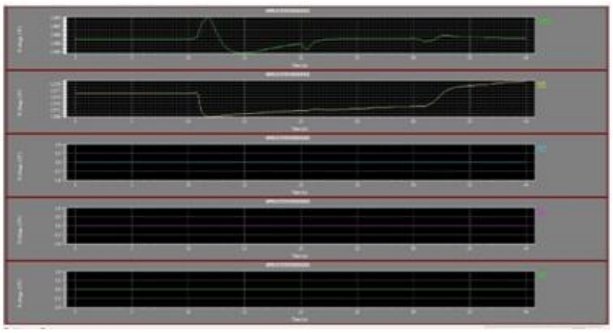

Figure.13.Simulation results of 6T ALU

Table.1.Power analysis for 3processors

TYPES OF PROCESSORS	NO.OF TRANSISTORS USED	POWER CONSUMED
BASIC ALU	1642	2.789961e-001 watts
REVERSIBLE ALU	2418	1.861542e-001 watts
REVERSIBLE ALU USING 6T ADDER	962	1.165185e-001 watts

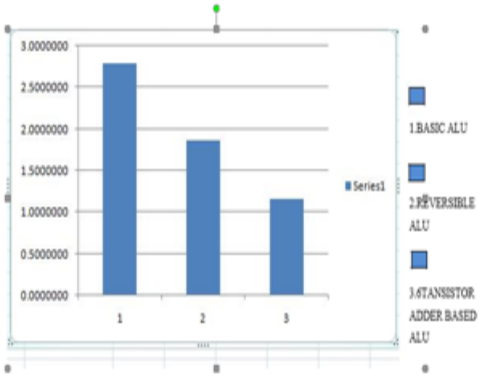

Figure.14. Bar graph representation for power

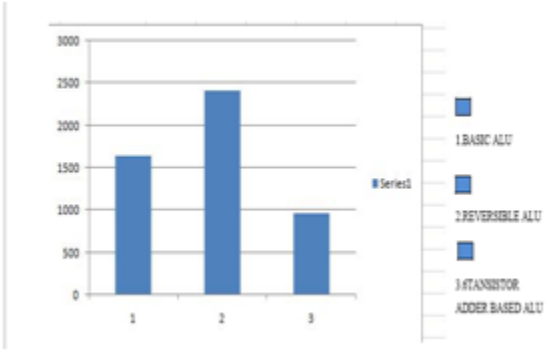

Figure.15. Bar graph representation for transistors used

V.CONCLUSION

In this work we designed a low power, low area arithmetic logic unit; various operations can be realized by using suitable control logic to one of the input variables of ripple carry adder. In this work ALU design based on reversible logic units with low power control unit for arithmetic and logical operations is proposed. In this we presented an approach to realize multipurpose binary reversible gates. Such gates can be used in regular circuits realizing Boolean functions. In the same way it is possible to construct multiple value reversible gates having similar properties. This proposed asynchronous design has application in building ALU, i.e. reversible processor. In this work we presented a novel ALU design using CMOS technology which comprises of 6T adder module which is consuming low area, low power compared to the normal ALU, reversible ALU.

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