ISSN XXXX XXXX © 2017 IJESC

Research Article Volume 7 Issue No.11

A L-K Equation is Implemented for Reducing Baseline Effect in UC-FinFET and Utilise Fluctuated Intrinsic LER

Hema Durga Aparna .Y[1], G. Madhusudhana Rao[2], C.Amala[3], P.Jayababu[4]
M. Tech Scholar[1], HOD[2], Assistant Professor[3, 4]
Department of ECE
Nannapaneni Venkat Rao College of Engineering and Technology, Tenali, India

Abstract:
This document tells about how to maintain constant Pulse current response and force of fin line-edge on the built-in variation of unconstructive capacitance in FinFETs by atomistic simulation attached with the Landau-Khalatnikov equation. We reduce baseline effect by using L-K equation. We narrative a feedback criterion stemming from the internal voltage amplification inherent in the unconstructive capacitance of voltage controlled Circuit. This feedback mechanism results in the superior protection to Fin-LER induced operating-voltage and internal processing-movements variations for Unconstructive-FinFETs as compared with the FinFET counterparts. This revision may provide insights for Circuit designs using unconstructive capacitance FETs.

Index Terms: Variability, Unconstructive Capacitance, FinFET, Fin-LER.

I.INTRODUCTION

It is crucial to reduce the power consumption. At Circuit level, the supply voltage reduction and leakage Pulse current minimization are vital requirements, which necessitate steep sub-operable-slope transistors such as tunnel FET (TFET), Tiny-electro-mechanical (NEM) FET, impact-ionization MOS (I-MOS) transistor and unconstructive capacitance FET (UCFET). The UCFET is in scrupulous one of the most promising steep slope Circuits and has garnered substantial interest recently. The phenomena of ferroelectric NC characteristics and sub-kT/q switching UCFETs with high ON/OFF Pulse current ratio had been experimentally demonstrated in several studies. To introduce NCFETs into the industry, it is important to push in the ferroelectric film in the mainstream Fin- FET technology, and ferroelectricity in doped hafnium oxide compatible with present high-k metal-gate process has been reported. For ultra low power steep-slope Circuits, intrinsic variation is a crucial issue. The fin line-edge roughness (Fin-LER) is one of the most important intrinsic variation sources for scaled FinFETs. How might the Fin-LER affect the unconstructive capacitance FinFET (UC-FinFET) has rarely been known and merits investigation. In this work, we report a feedback mechanism that may suppress the Fin-LER induced intrinsic variability in UC-FinFETs.

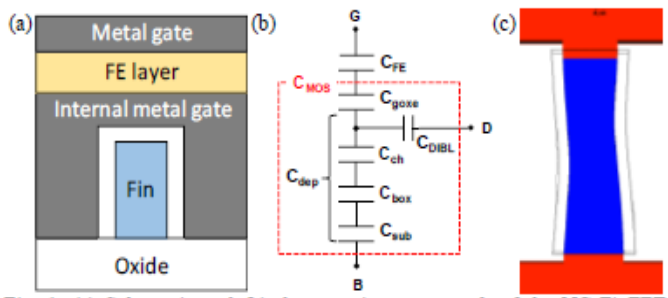

Fig. 1. (a) Schematic and (b) the capacitance network of the NC-FinFET structure in this work. (c) An instance of the baseline FinFETs that are affected by Fin-LER.

TABLE I
PHYSICAL AND GEOMETRICAL PARAMETERS FOR THE NOMINAL NC-FINFET

L_G	22 nm	Physical gate length
H_{fin}	25 nm	Fin height
W_{fin}	9.6 nm	Fin width
T_{gox}	2 nm	Front gate EOT
α	-1.3e11 V·cm/Coul	Doped HfO material parameter [16]
β	6.5e20 V·cm^5/Coul^3	Doped HfO material parameter [16]
γ	0	Doped HfO material parameter [16]
$Area_{FE}$	38.4 nm x 22 nm	Area of the ferroelectric layer
T_{FE}	12 nm	Thickness of the ferroelectric layer

II. CIRCUIT STRUCTURE AND SIMULATION SCHEME

To obtain the DC characteristics of the UC-FinFETs, we coupled the 3D TCAD atomistic simulation with the post-processed one-dimensional steady-state Lan-dau-Khalatnikov (L-K) equation as described by

$$V_{FE} = 2\alpha T_{FE} P + 4\beta T_{FE} P^3 + 6\gamma T_{FE} P^5 \quad (1)$$

Where VFE is the voltage across the ferroelectric layer and P is the polarization inside the ferroelectric layer which is approximately the charge density (QFE) on the ferroelectric capacitor. During the procedure, the drain Pulse current and the gate charge density at each bias point of the baseline FinFETs are extracted from the Aided DEsig simulation. The VFE corresponding to each bias and the transfer curves of the UC-FinFETs can then be obtained by replacing VG by VG + VFE. Pertinent physical and geometrical parameters for the doped hafnium oxide ferroelectric material and the nominal FinFET are listed in Table I. The thicknesses of the ferroelectric layer and the gate oxide are designed to avoid the ferroelectric hysteresis and to achieve sub-kT/q switching. Using the parameters and the simulation methodology aforementioned, the nominal transfer characteristics for the baseline FinFET and the UC-FinFET are depicted in Fig. 2 along with the Fin-LER induced dispersion curves. The sub operable swing values for the nominal FinFET and UC-FinFET are 90.8 and 48.8 mV/decade, respectively, and the ratio between the two is de-

termined by the internal voltage amplification (AV) from the unconstructive capacitance (CFE):

$$A_V = \frac{\partial V_{MOS}}{\partial V_G} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}(C_{DIBL})} \qquad (2)$$

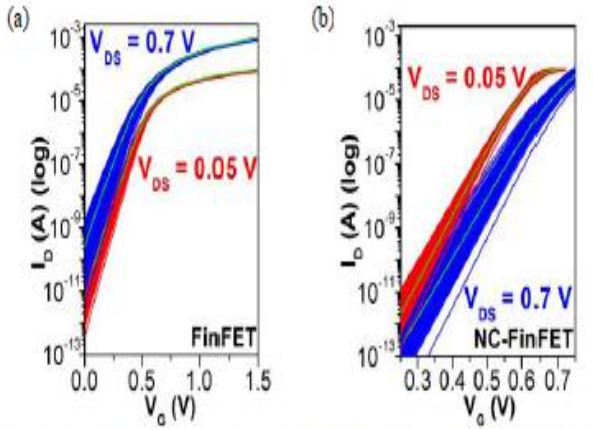

Fig. 2. Transfer curve dispersions for (a) the baseline FinFETs and (b) the NC-FinFETs under different drain biases (V_{DS}). The green curves are nominal cases.

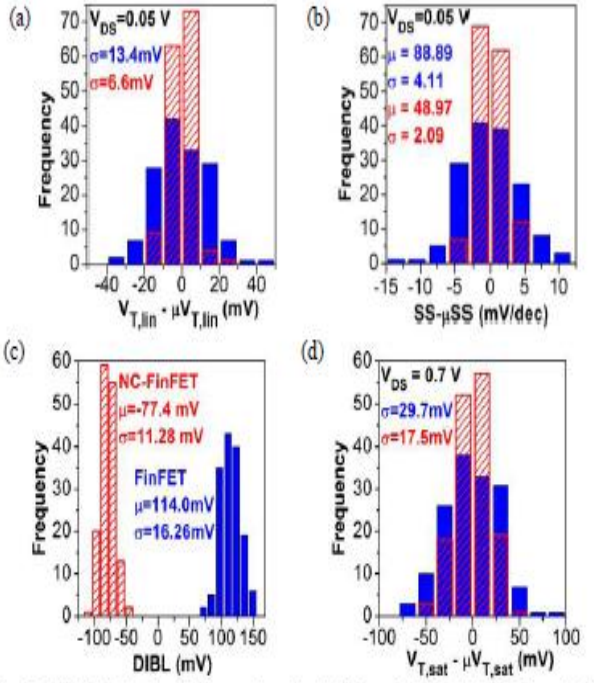

Fig. 3. Fin-LER induced dispersions in (a) $V_{T,lin}$, (b) SS, (c) DIBL and (d) $V_{T,sat}$. The blue bars and red hatched bars represent the FinFET and the NC-FinFET cases, respectively.

Where VG and VMOS denote the voltages of the external and internal metal gates, respectively, and CFE and CMOS are described in Fig. 1(b). Note that the total gate capacitance of the underlying FinFET, CMOS, is a function of the drain coupling, CDIBL We apply the one-dimensional Fourier synthesis technique with the Gaussian model to generate the roughness patterns of the side gates as an instance illustrated in Fig. 1(c) . The two side gates are assumed to be uncorrelated. The LER rms amplitude and the correlation length are defined as 1 nm and 15. nm, respectively. 150 samples are used for each case to acquire statistically reliable results. The operable voltage, VT, is determined by the constant Pulse current method, while the average sub operable swing, SS, is calculated within five orders of drain Pulse current.

III. RESULTS AND DISCUSSION

The Fin-LER affects the electrostatic integrity of the transistors as indicated by the transfer curve dispersions in Fig. 2. The short channel effects (SCEs) for the Circuits are dependent upon the fin width, resulting in the observed VT, SS and drain-induced-barrier-lowering (DIBL) variations. The sub-operable characteristics and their dispersions of the baseline FinFETs and the UC-FinFETs are benchmarked in this work. The VT, lin, SS, DIBL and VT, sat variability distributions are shown in Fig. 3. It can be seen that the UC-FinFETs possess better immunity (smaller σ) to the Fin-LER, which can be ex-plained by an unconstructive capacitance feedback mechanism.

$$\Delta V_{T,NC-FinFET} = \Delta V_{T,FinFET} \times \left(\frac{\partial V_G}{\partial V_{MOS}}\right) = \Delta V_{T,FinFET} \times A_V^{-1} \qquad (3)$$

$$SS_{NC-FinFET} = SS_{FinFET} \times \left(\frac{\partial V_G}{\partial V_{MOS}}\right) = SS_{FinFET} \times A_V^{-1} \qquad (4)$$

Eqn. (4) indicates that the voltage amplification AV is still the key to the reduced SS variability for the UC-FinFET in Fig. 3(b). Note that the AV depends on the drain coupling CDIBL (see Eqn. (2)). As CDIBL increases, AV increases because of the in-crease in CMOS (see Fig. 1(b)) [23]. In other words, considering Fin-LER, the Circuit instance with larger CDIBL (and thus larger SS FinFET) will possess a larger AV, and vice versa. This explains the improved μ/σ ratio in SS for the UC-FinFET in Fig. 3(b).

IV. CONCLUSION

Compared the impact of Fin-LER on the intrinsic variability of UC-FinFETs and the underlying FinFETs by TCAD atomistic simulation coupled with the L-K equation. Our study indicates that, outstanding to the internal voltage amplification natural in the unconstructive capacitance FET, a feedback mechanism that may affect the intrinsic variability exists in the UC-FinFET. This feedback mechanism leads to the better immunity to Fin-LER induce variation for the UC-FinFET. Reduced base line effect in Fin Fet.

V. REFERENCES

[1]. R. Aitken, V. Chandra, J. Myers, B. Sandhu, L. Shifren and G. Yeric, "Circuit and technology implications of the Internet of Things," *Proc. VLSI Technol. Symp.*, Jun. 2014, pp. 1–4, doi: 10.1109/VLSIT.2014. 6894339.

[2]. M. B. Taylor, "Is dark silicon useful? Harnessing the four horsemen of the coming dark silicon apocalypse," *DAC Design Automation Conf. 2012*, Jun. 2012, pp. 1131–1136.

[3]. W. Y. Choi, B.-G. Park, J. D. Lee and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with suboperable swing (SS) less than 60 mV/dec," *IEEE Electron Circuit Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007, doi: 10.1109/ LED. 2007.901273.

[4]. A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for be-yond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010, doi: 10.1109/ JPROC. 2010. 2070470.

[5]. A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as ener-gy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011, doi: 10.1038/nature10679.

[6]. H. Kam, D. T. Lee, R. T. Howe and T.-J. King, "A new Tiny-electro-mechanical field effect transistor (NEMFET) design for low-power elec-tronics," *IEDM Tech. Dig.*, Dec. 2005, pp. 463–466, doi: 10.1109/IEDM. 2005.1609380.

[7]. K. Gopalakrishnan, P. B. Griffin and J. D. Plummer, "I-MOS: a novel semiconductor Circuit with a suboperable slope lower than kT/q," *IEDM Tech. Dig.*, Dec. 2002, pp. 289–292, doi: 10.1109/IEDM.2002.1175835.

[8]. S. Salahuddin and S. Datta, "Use of unconstructive capacitance to provide voltage amplification for low power Tinyscale Circuits," *Tiny Lett.*, vol. 8, no. 2, pp. 405–410, Feb. 2008, doi: 10.1021/nl071804g.

[9]. A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh and S. Salahuddin, "Unconstructive capacitance in a ferro-electric capacitor," *Nature Materials*, vol. 14, no. 2, pp. 182–186, Feb. 2015, doi: 10.1038/nmat4148.

[10]. W. Gao, A. Khan, X. Marti, C. Nelson, C. Serrao, J. Ravichandran, R. Ramesh and S. Salahuddin, "Room-temperature unconstructive capacitance in a ferroelectric-dielectric super lattice heterostructure," *Tiny Lett.*, vol. 14, no. 10, pp. 5814–5819, Sep. 2014, doi: 10.1021/nl502691u.

[11]. A. Rusu, G. A. Salvatore, D. Jiménez and A. M. Ionescu, "Met-al-ferroelectric-metaoxide-semiconductor field effect transistor with sub-60mV/decade suboperable swing and internal voltage amplifica-tion," *IEDM Tech. Dig.*, Dec. 2010, pp. 16.3.1–16.3.4, doi: 10.1109/ IEDM.2010.5703374.

[12]. K.-S. Li, P.-G. Chen, T.-Y. Lai, C.-H. Li, C.-C. Chen, C.-C. Chen, Y.-J. Wei, Y.-F. Hou, M.-H. Liao, M.-H. Lee, M.-C. Chen, J.-M. Sheih, W.-K. Yeh, F.-L. Yang, S. Salahuddin and C. Hu, "Sub-60mV-swing unconstructive capacitance FinFET without hysteresis," *IEDM Tech. Dig.*, Dec. 2015, pp. 22.6.1–22.6.4, doi: 10.1109/IEDM.2015.7409760.

[13] A.I. Khan, K. Chatterjee, J. P. Duarte, Z. Lu, A. Sachid, S. Khandelwal, R. Ramesh, C. Hu and S. Salahuddin, "Unconstructive capacitance in short-channel FinFETs externally connected to an epitaxial ferroelectric capacitor," *IEEE Electron Circuit Lett.*, vol. 37, no. 1, pp. 111–114, Jan. 2016, doi: 10.1109/LED. 2015.2501319.

[14]. M. H. Lee, S.-T. Fan, C.-H. Tang, P.-G. Chen, T.-C. Chou, H.-H. Chen, J.-Y. Kuo, M.-J. Xie, M.-H. Liao, C.-A. Jong, K.-S. Li, M.-C. Chen and C. W. Liu, "Physical thickness 1.x nm ferroelectric HfZrOx negative ca-pacitance FETs," *IEDM Tech. Dig.*, Dec. 2016, pp. 12.1.1–12.1.4, doi: 10.1109/ IEDM.2016.7838400.

[15]. E. Ko, J. W. Lee and C. Shin, "Unconstructive capacitance FinFET with sub-20-mV/decade sub operable slope and minimal hysteresis of 0.48 V," *IEEE Electron Circuit Lett.*, vol. 38, no. 4, pp. 418–421, April 2017, doi: 10.1109/LED.2017.2672967.

[16]. T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder and U. Böttger, "Fer-ro electricity in hafnium oxide thin films," *Appl. Physics Lett.*, vol. 99, no. 10, pp. 102903, Sep. 2011, doi: 10.106 3/1.3634052.

[17]. K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. Mclntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes,M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S.Williams and K. Zawadzki, "A 45 nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging," *IEDM Tech. Dig.*, Dec. 2007, pp. 247–250, doi: 10.1109/ IEDM.2007. 4418914.

[18]. A. Asenov, A. R. Brown, J. H. Davies, S. Kaya and G. Slavcheva, "Simulation of intrinsic parameter fluctuations in decaTinymeter and Tinymeter-scale MOSFETs," *IEEE Trans. Electron Circuits*, vol. 50, no. 9, pp. 1837–1852, Sep. 2003, doi: 10.1109/TED.2003.815862.

[19]. E. Baravelli, A. Dixit, R. Rooyackers, M. Jurczak, N. Speciale and K. De Meyer, "Impact of line-edge roughness on FinFET matching performance," *IEEE Trans. Electron Circuits*, vol. 54, no. 9, pp. 2466–2474, Sep. 2007, doi: 10.1109/TED.2007.902166.

[20]. T. Skotnicki, C. Fenouillet-Beranger, C. Gallon, F. Boeuf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, S. Clerc, M. Sellier, A. Cathignol, J.-P. Schoellkopf, E. Perea, R. Ferrant and H. Mingam, "Innovative Materials, Circuits, and CMOS Technologies for Low-Power Mobile Multimedia," *IEEE Trans. Electron Circuits*, vol. 55, no. 1, pp. 96-130, Jan. 2008. doi: 10.1109/TED.2007.911338

[21]. C. Hu, S. Salahuddin, C. I. Lin and A. Khan, "0.2V adiabatic UC-FinFET with 0.6mA/μm ION and 0.1nA/μm IOFF," *Proc. 73rd Annu. Circuit Re-search Conf. (DRC)*, Jun. 2015, pp. 39–40, doi: 10.1109/DRC.2015. 7175542.

[22]. Sentaurus TCAD, G2012-06-SP2 Manual.

[23]. C.-P. Tsai and P. Su, "New findings on the gate-length dependence of suboperable swing for ultra-thin-body unconstructive capacitance FETs," *Ex-tended Abstracts of the 2016 International Conference on Solid State Circuits and Materials (SSDM)*, Tsubaka, Japan, Sep. 2016, pp. 19–20.