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Characterization of A Novel Low Power and Area Efficient 13t SRAM Cell

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Abstract:
Scaling of CMOS technology creates new challenges to the SRAM circuit design, mainly leakage power and stability. A new seven transistor SRAM (7T) is in this paper which eliminates the stability issues, reliable write and has a reduced cell area. Leakage current in 7T SRAM cell without Super cut-off word lines is almost same as in 6T SRAM cell and 7T SRAM cell with super cut-off word lines is reduced by 26% of leakage power present in 8T SRAM cell. Compared to the conventional 7T, 8T SRAM cell with proposed 13TSRAM has reduced delay, power consumption. The proposed 13T SRAM is compared with existing 7T, 8T SRAM cells in 180nm technology. The Overall performance of proposed 13T is best among the 7T, 8T, 13T.

Index Terms: SRAM memory cell, Data Stability.

1.INTRODUCTION

SRAM is the most widely used memory cell architecture in present day memories. In each new technology generation, the supply voltage reduces which results in degradation of data stability. Process variations in CMOS technologies also affect the SRAM cell stability. This issue has to be taken care while designing high-density memories. Existing 7T improves stability but the leakage current is more when compared to 6T and the data stability during write operation is less. Leakage current is another factor because in high density memory circuits, most of the memory cells are in idle state except for the few cells to perform read or write operation. The only source of energy consumption in an idle state is leakage. So, a low power-hungry SRAM cell architecture is the need of the hour in System-On-Chips (SoC) and high performance microprocessors as device scaling is power constrained. 8T and 9T SRAM cell improves data stability during write, but fails to reduce leakage current. More than 9 Transistor SRAM cells reduce the leakage current but occupy more area per cell. Considering the major drawbacks like unreliable read in 6Tlarge area per cell in 8T, the considerably high leakage power in existing 7T and 8T memory cells, an area efficient, low-leakage memory cell is needed which can perform reliable read and write operations. An area efficient seven-transistor (7T) SRAM cell with enhanced data stability and reduced leakage current is proposed in this paper. Existing 7T has only one access transistor. During write operation, only bitline or bitline bar current will charge or discharge through it, but there is no guarantee that the bit line and bitline bar will be switched. These results in wrong data being stored in the storage nodes during write operation. Proposed architecture has two access transistors. In write operation, if bit line is charging through an access transistor, then the bitline bar will discharge through the other access transistor. It ensures reliable write operation. Cell area is minimized by using smaller device dimensions for back to back connected inverters. Leakage power reduced in a SRAM cell by minimizing sub-threshold leakage current. Read delay is reduced by discharging read bitline voltage through a single transistor instead of two transistors.

2. EXISTING SYSTEM

7T SRAM

7T SRAM cell in a 180nmCMOStechnology is shown in Fig. 1 with sizing of individual transistor and current does not flow from RV_{DD} to RBL. So, the voltage in RBL remains at logic 0. This RBL voltage ensures logic 1 to be stored in the cell. Read delay is small because time constant is small. To further reduce the delay, P_3 is designed with high W/L ratio. Write Operation: During write operation, WRSIG =1, Rvdd=0 and RBL is at logic zero. Assume that node Qis storing logic 1 and node *Qbar* has logic 0. Write logic 0 into a storage node Q, *BLbar* is clamped to logic 1 and BL is clamped to logic 0. Node voltage Q discharges through $P_1$and N_4 and *Qbar* charges through N_3 and N_2. When charging and discharging node voltage characteristics cross each other, flipping of stored value occurs. Then Q becomes logic 0.

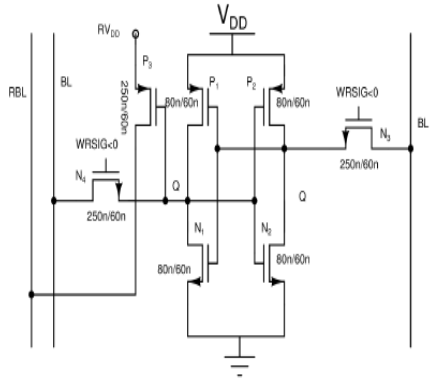

Figure.1. schematic of 7T SRAM

8TSRAM

In this work we propose a single ended 8T SRAM design as shown in Figure 8 that enhances data stability by improving the Read Static Noise Margin and also reduces the Power Consumption. In this design, a transmission gate is used for Read purpose. The additional signal RWLB is an inversion signal of read wordline (RWL). It controls the additional transistor M7 of the transmission gate. While the RWL and RWLB are asserted and once the transmission gate is ON, astored node is connected to RBL. Thus a stored value at Q is being transferred to or read through RBL. One of the major advantages of this design is that it is not necessary to prepare a Precharge circuit as required in prior 8T SRAM cell and a sense amplifier circuit as required in 6T SRAM cell because the stored value is directly passed through transmission gate. A charge/discharge power on the RBL is consumed only when the RBL is changed. Consequently, no power is dissipated on the RBL if an upcoming data is the same as the previous state. The design reduces a bitline power in both cases that the consecutive "0"s and consecutive "1"s are read out.

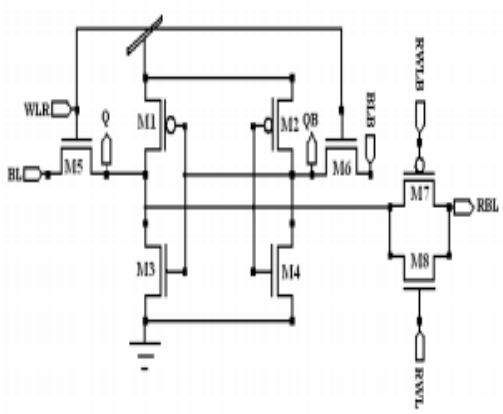

Figure.2. schematic of 8T SRAM

3.PROPOSEDSYSTEM

Bitcell Design SRAM design for low-voltage operation has become increasingly popular in the recent past. Various bitcell designs and architectural techniques have been proposed to enable operation deep into the subthreshold region .These designs generally incorporate the addition of a number of transistors into the bitcell topology, compared with the baseline 6T SRAM bitcell, trading off density with robust, low-voltage functionality. However, these bitcells were designed for operations under standard operating environments, and thereby, do not provide sufficient robustness to SEUs under high-radiation conditions. In addition, the design architecture of these cells is based on the standard 6T cell; therefore, the 6T cell has the same hardening ability to most, if not all, these unprotected cells. As shown in Section II, the radiation hardening ability of the 6T cell is extremely low,especially when compared with radiation hardening solution designs. The proposed bitcell is specifically designed to enable robust, low-voltage, ULP operation in space applications and other high-radiation environments. This is achieved by employing a dual-feedback, separated-feedback mechanism to overcome the increased vulnerability due to supply voltage scaling. The schematic representation of the proposed 13T bitcell is shown in Fig. 2. The storage mechanism of this circuit comprises five separate nodes: Q, QB1, QB2, A, and B, with the acute data value stored at Q. This node is driven by a pair of CMOS inverters made up of transistors N3, P3, N4, and P4 that are, respectively, driven by the inverted data level, stored at QB1 and QB2. QB1 and QB2 are, respectively, driven to VDD or GND through devices P1, P2, N1, and N2 that are controlled by the weak feedback nodes A and B that are connected to Q through a pair of complementary devices (P5 and N5) gated by QB2. By driving the acute data level by a pair of equip potentially driven, but independent, inverters, a strong, dual-driven feedback mechanism is applied with node separation for SEU protection.

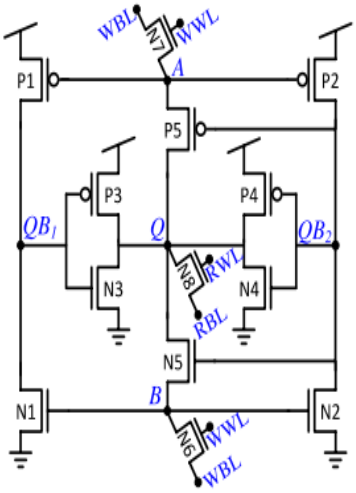

Figure.3. Schematic of the proposed 13T SRAM bitcell

4. SIMULATION AND RESULT

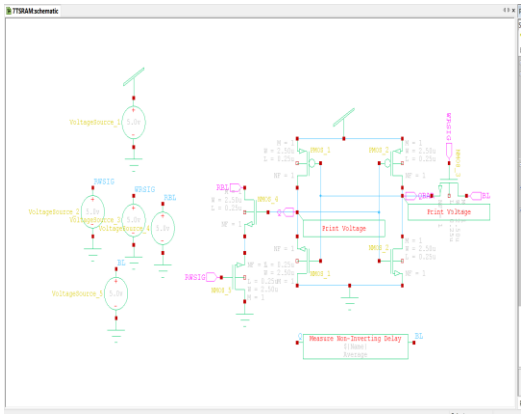

Figure.4. schematic of 7T SRAM

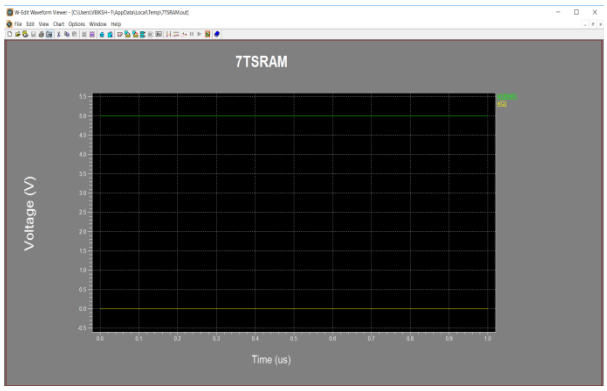

Figure.5. waveformof 7T SRAM

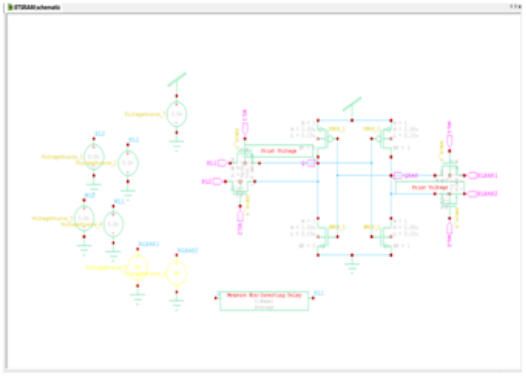

Figure.6. schematic of 8T SRAM

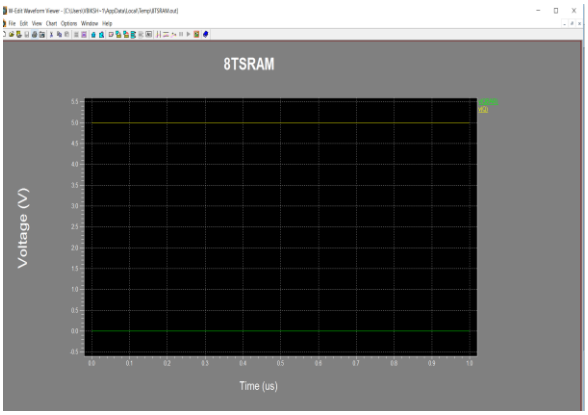

Figure.7. waveformof 8T SRAM

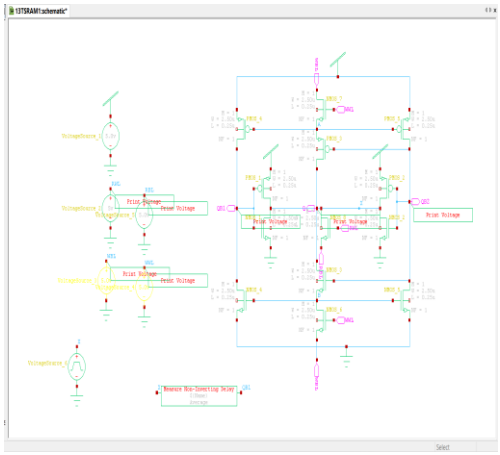

Figure.8. schematic of 13T SRAM

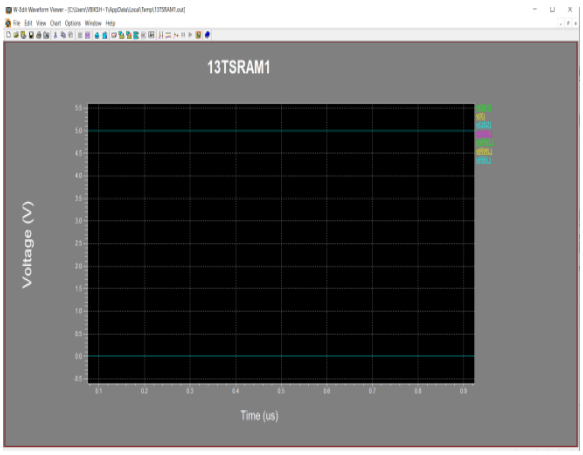

Figure.9. waveformof 13T SRAM

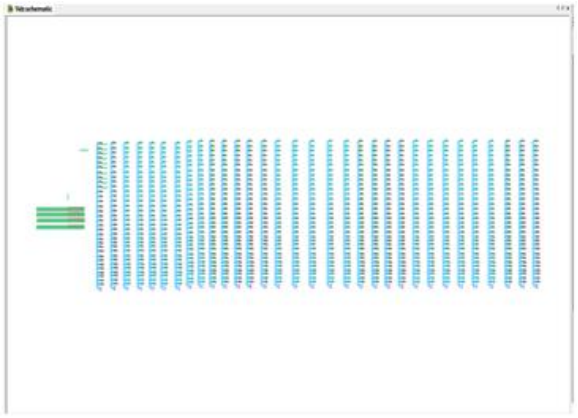

Figure.10. schematic of 1KB 13T SRAM

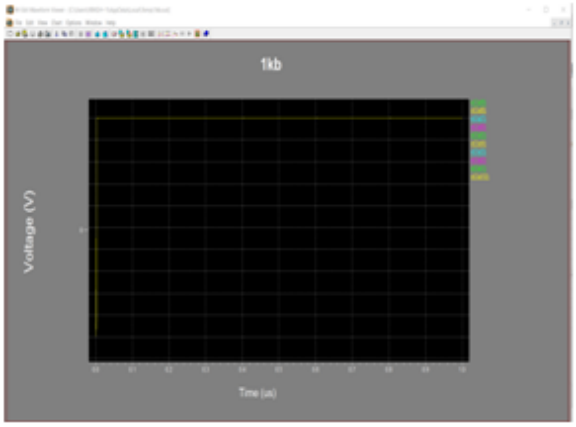

Figure.11. waveformof 1KB 13T SRAM

Table.1. Comparison between Proposed and Existing.

SRAM	POWER	DELAY
6T	1.52E-02	2.50E-12
7T	6.08E-07	4.84E-08
8T	1.52E-02	3.29E-12
13T	3.40E-06	1.07E-09
13T 1KB	4.82E-03	

5.CONCLUSION

This paper proposed a 13T SRAM bitcell, designed for robust, low-voltage, ULP operation in high-radiation environments, such as those encountered by space applications

6. REFERENCE:

[1].A. Wang, B. H. Calhoun, and A. P. Chandrakasan, Sub-Threshold Design for Ultra Low-Power Systems (Series on Integrated Circuits and Systems). Secaucus, NJ, USA: Springer-Verlag, 2006.

[2].S. Fisher, A. Teman, D. Vaysman, A. Gertsman, O. Yadid-Pecht, and A. Fish, "Digital subthreshold logic design—Motivation and challenges," in Proc. IEEE Conv. Elect. Electron. Eng. Israel (IEEEI), Dec. 2008, pp. 702–706.

[3].T. Heijmen, D. Giot, and P. Roche, "Factors that impact the criti-cal charge of memory elements," in Proc. IEEE Int. On-Line Test.Symp. (IOLTS), Jul. 2006, pp. 1–6.

[4].R. C. Baumann, "Radiation-induced soft errors in advanced semicon-ductor technologies," IEEE Trans. Device Mater. Rel., vol. 5, no. 3,pp. 305–316, Sep. 2005.

[5].T. Karnik and P. Hazucha, "Characterization of soft errors caused by single event upsets in CMOS processes," IEEE Trans. Dependable Secure Comput., vol. 1, no. 2, pp. 128–143, Apr./ Jun. 2004.

[6].P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," IEEE Trans. Nucl. Sci., vol. 50, no. 3, pp. 583–602, Jun. 2003.

[7].P. E. Dodd and F. W. Sexton, "Critical charge concepts for CMOS SRAMs," IEEE Trans. Nucl. Sci., vol. 42, no. 6, pp. 1764–1771, Dec. 1995.

[8].C. Detcheverryet al., "SEU critical charge and sensitive area in a submicron CMOS technology," IEEE Trans. Nucl. Sci., vol. 44, no. 6, pp. 2266 –2273, Dec. 1997.

[9].J. L. Barth, C. S. Dyer, and E. G. Stassinopoulos, "Space, atmospheric, and terrestrial radiation environments," IEEE Trans. Nucl. Sci., vol. 50, no. 3, pp. 466–482, Jun. 2003.

[10].M. A. Bajuraet al., "Models and algorithmic limits for an ECC-based approach to hardening sub-100-nm SRAMs," IEEE Trans. Nucl. Sci., vol. 54, no. 4, pp. 935–945, Aug. 2007.

[11].L. Sterpone and M. Violante, "Analysis of the robustness of the TMR architecture in SRAM-based FPGAs," IEEE Trans. Nucl. Sci., vol. 52, no. 5, pp. 1545–1549, Oct. 2005.

[12].E. H. Cannon, D. D. Reinhardt, M. S. Gordon, and P. S. Makowenskyj, "SRAM SER in 90, 130 and 180 nm bulk and SOI technologies," in
Proc. IEEE Int. Rel. Phys. Symp., Apr. 2004, pp. 300–304.

[13].T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," IEEE Trans. Nucl. Sci., vol. 43, no. 6, pp.2874–2878, Dec. 1996.

[14]. ITRS. (2013). International Technology Roadmap for Semiconductors —2013 Edition. [Online]. Available: http:// www.itrs.net

[15].B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation," IEEE J. Solid-State Circuits, vol. 42, no. 3, pp. 680–688, Mar. 2007.

[16].B. H. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and sizing for minimum energy operation in subthreshold circuits," IEEEJ. Solid-State Circuits, vol. 40, no. 9, pp. 1778–1786, Sep. 2005.

[17].E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," IEEE J. Solid-State Circuits, vol. 22, no. 5, pp. 748–754, Oct. 1987.

[18].A. Teman, L. Pergament, O. Cohen, and A. Fish, "A 250 mV 8 kb 40 nm ultra-low power 9T supply feedback SRAM (SF-SRAM)," IEEEJ. Solid-State Circuits, vol. 46, no. 11, pp. 2713–2726, Nov. 2011.

[19].J. Mezhibovsky, A. Teman, and A. Fish, "Low voltage SRAMs and the scalability of the 9T supply feedback SRAM," in Proc. IEEE Int.Syst.-Chip Conf. (SOCC), Sep. 2011, pp. 136–141.

[20].N. Verma and A. P. Chandrakasan, "A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy," IEEE J. Solid-StateCircuits, vol. 43, no. 1, pp. 141–149, Jan. 2008.

[21].I. J. Chang, J.-J. Kim, S. P. Park, and K. Roy, "A 32 kb 10T sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 650–658, Feb. 2009.

[22].J. Wang, S. Nalam, and B. H. Calhoun, "Analyzing static and dynamic write margin for nanometer SRAMs," in Proc. ACM/IEEE Int. Symp.Low Power Electron. Design (ISLPED), Aug. 2008, pp. 129–134.

[23].G. R. Srinivasan, P. C. Murley, and H. K. Tang, "Accurate, predictive modeling of soft error rate due to cosmic rays and chip alpha radiation," in Proc. IEEE Int. Rel. Phys. Symp., Apr. 1994, pp. 12–16.

[24].S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant 10T SRAM bit-cell with differential read capability," IEEE Trans. Nucl.Sci., vol. 56, no. 6, pp. 3768–3773, Dec. 2009.