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Design and Implementation of High Performance Vedic Multiplier using Brent Kung Adder

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Abstract:
In VLSI design, the performance of any system is determined by the performance of the element si.e. Multiplier. Multiplier is one of the most important parts in any processor speed which improves the speed of the operation for example in special application processors like Digital Signal Processor (DSPs). Basically, the operational speed of any digital signal processor is strictly dependent upon the speed of the multipliers used. Here, we have used Urdhva Tiryakbhyam method of ancient Vedic mathematics which is derived from the ancient Vedic sutras and booth algorithm method. Vedic mathematics with less number of bits can be used to implement multiplier efficiently in signal processing algorithms. Vedic Mathematics provides principles of high speed multiplication. Here, in this paper we are trying to design high speed Vedic multiplier considering two methodologies (Vedic multiplier using Mux based adder and Vedic multiplier using Brent Kung adder) which are discussed and compared on the basis of their performance and results. Proposed design is simulated using ISim and synthesized using Xilinx ISE 14.5. When compared with Mux based Vedic multipliers, proposed design shows a significant improvement in speed.

Keywords: Vedic Multiplier, Delay, speed, BrentKung adder, Urdhva Tiryagbhyam Sutra, Verilog HDL

1. INTRODUCTION

Multipliers are frequently used in DSP, image processing architectures and microprocessors. It plays an important fundamental function in arithmetic operations. These days in modern VLSI design delay in data path is considered as a critical parameter. In present time designers are demanding high speed of operation, so it is essential to minimize the delay. There has been lot of researches and work to reduce the delay and now designers have shifted their focus on making a multiplier circuit which are efficient and considerably faster. A high speed processor performance greatly depends on the multiplier, in most digital signal processing systems as well as in all-purpose processors which is one of the essential hardware components also it's consumed area is more. Vedic multiplier gives the fast speed of operations than the conventional multiplier and requires less system memory. As compared to other multiplier design this multiplier requires very small area. Here in this work we use Brent Kung adder for designing Vedic multiplier. Brent Kung adder is the parallel prefix form of carry look ahead adder. In this paper 16-bit Vedic multiplier using Brent Kung adder has been designed The results shows that the proposed 16- bit Vedic multiplier is faster than 16- bit Vedic multiplier with MUX based adder. The reduction in the delay is approximately 30.6%. The main purpose of this work is to design and implement a high speed 16 X 16 bit Vedic multiplier by combining the best technique in Vedic mathematics named Urdhva Tiryagbhyam and Brent Kung adder.

2. VEDIC MATHEMATICS

The ancient Indian Vedic mathematics is now currently used in our global silicon chip technology for easier and faster calculations. The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). By using three sutras of Vedic mathematics the complex number multiplication can be done, which are Urdhva Tiryakbhyam sutra, Ekadhikena Purvena, and Nikhilam Navatascaraman Dasatah or simply Nikhilam. The Nikhilam sutra of Vedic mathematics can only be applied to large number multiplication. While the Urdhva Tiryakbhyam method of Vedic mathematics can be efficiently applied to all cases of multiplication. This is a universal method for obtaining fast multiplication which can be applied everywhere. It is very simple and easy to implement. For the multiplication of two numbers in the decimal number system these Sutras have been traditionally used. In this present work, we apply the same ideas to the binary number system for making the proposed algorithm compatible with the digital hardware.

2.1. Urdhva Tiryagbhyam

Urdhva Tiryakbhyam Sutra is a general multiplication formula which is applicable to all cases of multiplication. It literally means "Vertically and crosswise". This Sutra has been conventionally used for multiplication of two numbers in the decimal number system. The same idea has been applied for binary multiplication in this work. By breaking into smaller sizes, this can solve the multiplication of larger number (N X N bits). The 2 x 2 Vedic multiplier are basic building module through which higher multiplier are designed by splitting into smaller sizes.

This algorithm can be implemented into three steps which are as follows:

Step-1: The first step is vertical multiplication of LSB of both multiplicands.

Step-2: Second step is crosswise multiplication and additions of the partial products.

Step-3: Third step is vertical multiplication of MSB of the multiplicand and

addition with the carry propagated from step 2. For better understanding consider 2-bit two binary number are a1a0 and b1b0. The below figure 1 shows the 2 bit multiplier.

The expression of two bit Vedic multiplier is:

s0 = a0 and b0

s1 = (a1and b0) XOR (a0and b1)

c1 = (a1and b0) and (a0and b1)

s2 = c1 XOR (a1and b1)

c2 = c1 and (a1and b1)

sum = {c2,s2,s1,s0}

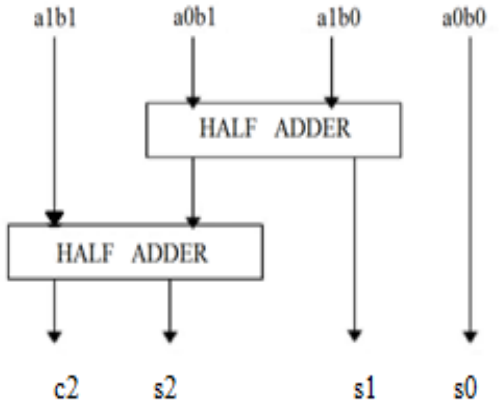


Figure.1.LineDiagramfor2 X2 Bitbinary multiplication using Urdhva Tiryagbhyam Sutra

a) Algorithm for 16 X 16 Bit binary numbers Multiplication Using Urdhva Tiryagbhyam:

A=A15A14A13A12A11A10A9A8 A7A6A5A4A3A2A1A0

X1 X0

B=B15B14B13B12B11B10B9B8 B7B6B5B4B3B2B1B0

Y1 Y0

X1X0

*Y1Y0

FEDC

CP= X0*Y0=C

CP=X1*Y0+X0*Y1=D

CP=X1*Y1=E

Where CP=Cross product

3. Brent Kung adder

Brent Kung adder is the type of parallel prefix adder. Parallel prefix adder are high performance carry tree adder in which pre-computing of propagation and generation signal take place. Due to the complexity (log2n) delay through the carry path, the parallel-prefix tree adders are more favourable in terms of speed as compared to other adders. It consumed less area and has maximum depth. The number of cell of Brent Kung adder can be calculated by (2n-1) –log2n and the delay of the structure is (2log2 n-2). The three steps are generally used for design a Brent Kung adder:

Step-1: It involves the creation of generate and propagate signals for the input operand bits.

Step-2: This involves the generation of carry signals.

Step-3: In this step the sum bits of the adder following stages of the operand bits and the preceding stage carry bit using a XOR gate

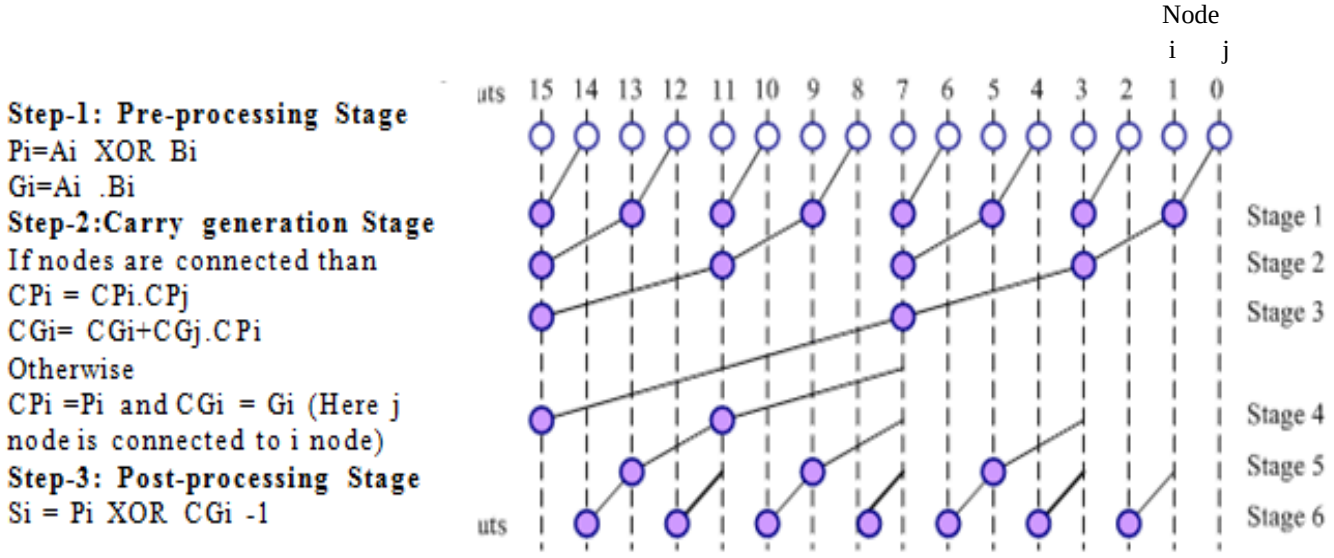


Figure.2. Schematic of 16 bit Brent Kung adder

4. Design of 16x16VedicMultiplierusingBrent Kung adder

The2x2-bitVedicmultiplier is the basic building section for the system. Two Halfad ders are required in designing 2x2 Vedic Multiplier. The4 x 4-bit multiplier is designed by using four2 x 2-bit Vedic multiplier. The 8x8bit Vedic multiplier is designed by using four 4x4bitVedicmultiplier building blocks. The approach applied for designing a16x16-bitVedic multiplier by using four 8x8 bit multiplier blocksandthree16-bit Brent Kungad der blocks is shown in figure 3.

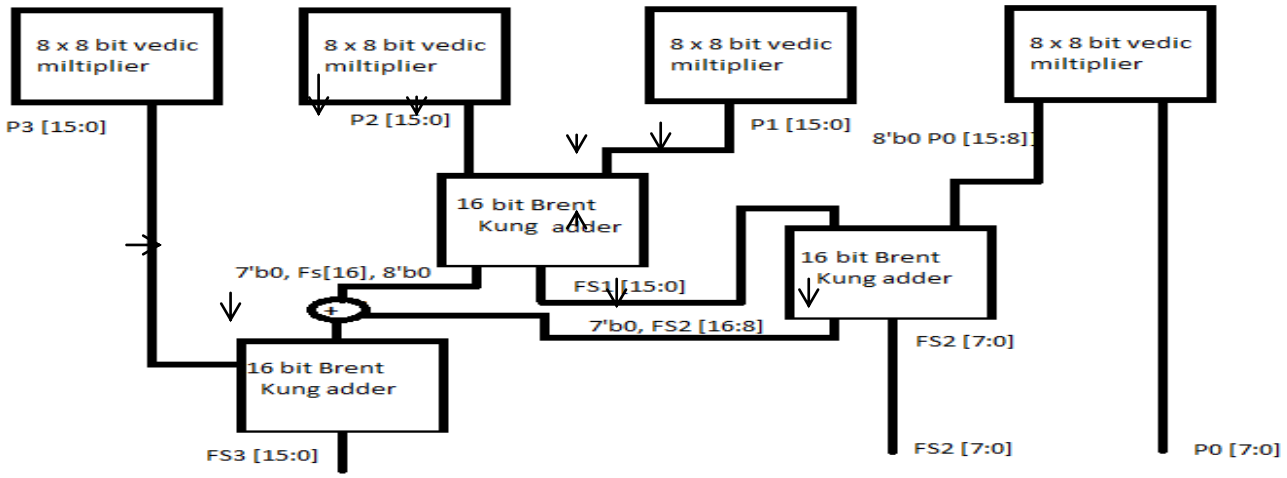
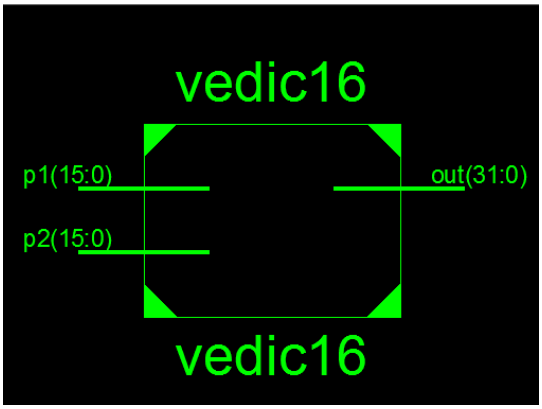


Figure.3.Block diagram of 16 x 16 bit Vedic Multiplier using Brent Kung adder

5. RESULT

5.1 Synthesis

The Verilog code of proposed Vedic multipliers (using Brent Kung adder) and Vedic multiplier using MUX based adder are syn the size dusing XILINX ISE 14.5.Thefigure4 &5 shows the RTL diagrams of both multipliers.



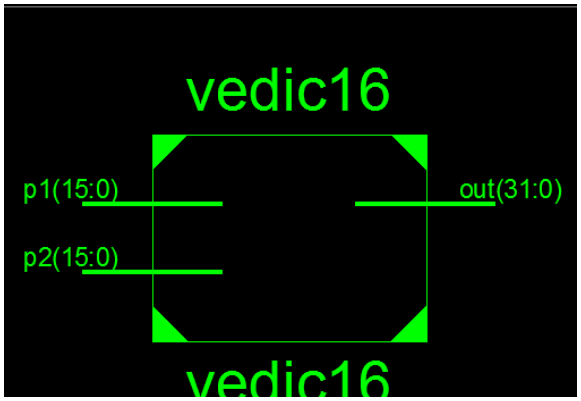


Figure.4. RTLviewof16x16Vedicmultiplier using Brent Kung adder Figure. 5.RTLviewof16x16Vedicmultiplier using

5.2. Simulation

The functionality of Vedic multiplier is verified and confirms the operation of the design from the simulated waveforms. The combinational delay is reduced drastically with a little bit of trade off in terms of area. ISim simulator is used for simulation purpose. Figure 6 & 7 shows the Simulation result for 16 bit Vedic multiplier in which 'P1' and 'P2'aresame set of inputs and 'out' is their product and table 1 gives the delay and number of slice LUTs comparison between these two design architecture.

a) Simulation of 16 X 16 bit Vedic Multiplier using Brent Kung adder The Simulation Result of 16X 16 bit Vedic Multiplier using Brent Kung adder are shown in figure 6 and Simulation result for 16 X 16-bit Vedic multiplier using MUX based adder is shown in figure 7 in which P1= 1111000000000000 and P2= 1000111111111111 is taken and result out =10000111000000000000000000000000 is obtained. Figure 8 gives the delay compression between two Vedic multiplier architecture designs.

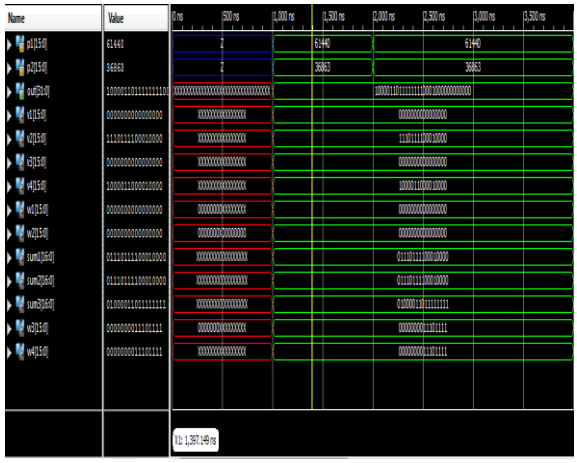


Figure.6. Simulation Result of 16X16 bit Vedic Multiplier using Brent Kung adder

Figure 7: Simulation Result of 16X16 bitVedic Multiplier using Mux based adder using Brent Kung adder

Table 1:

Type	No. of Bits	No.of bondedIOs	Delay (ns)	Level of logic	Number of Slice LUTs
Vedic multiplier usingBrent Kung adder	16	64	12.818	22	568
Vedic multiplier usingMUX basedadder	16	64	16.142	23	513

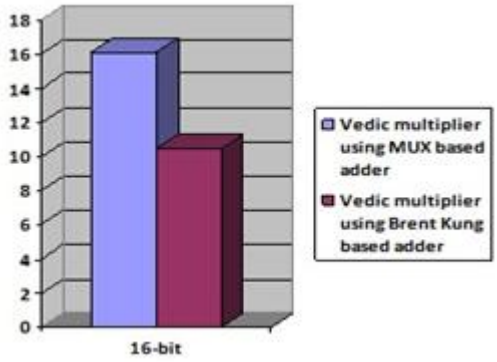


Figure.7.Delay compression between two Vedic multiplier

6. Conclusion and Future Work

This paper work presents a high performance design for multiplication by combining the feature of Vedic mathematics and Brent Kung adder. When we compared our purposed design with Vedic multipliers using Mux based adder proposed design gives much less delay. We conclude that the proposed Vedic multiplier is approximately 30.6% faster from the Vedic Multiplier using MUX based adder. The multiplier architecture and fast performance makes this particularly attractive for VLSI implementations. For future work, its performance within MAC unit and ALU can be tested and compared with other conventional and Vedic designs. This 16 bit Multiplier can be further extended to 32 bit or 64 bit multiplier.

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