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Reducing Power, Delay and Area of Threshold Logic by using D-Flip Flop

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Abstract:
In this paper, we describe a new approach of reduce dynamic power, leakage, and area. We first describe a new robust, standard-cell library of configurable circuits for implementing threshold functions. Abstractly, the threshold gate behaves as a multi-input, single-output, edge-triggered flip-flop, which computes a threshold function of the inputs on the clock edge. A new sense-amplifier-based flip-flop is presented. The output latch of the proposed circuit can be considered as between the standard NAND-based set/reset latch. The proposed provides design, reduced short-circuit power dissipation, and glitch-free operation.

1. INTRODUCTION

Exploitation of very large scale integration (VLSI) technology has developed to the point where millions of transistor can be implemented on a single chip. Complementary metal oxide semiconductor (CMOS) has been the backbone in mixed signal because it reducing power and providing good mix component for analog and digital design. Power consumption is one of the top issues of VLSI circuit design, for which CMOS is the primary technology. Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before the mobile era, power consumption has been a fundamental problem. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay and area and thus, designers are required to choose appropriate techniques that satisfy application and product needs. In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor. When it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limits the application of each technique. We propose a new approach, thus providing a new choice to low leakage power VLSI designers.

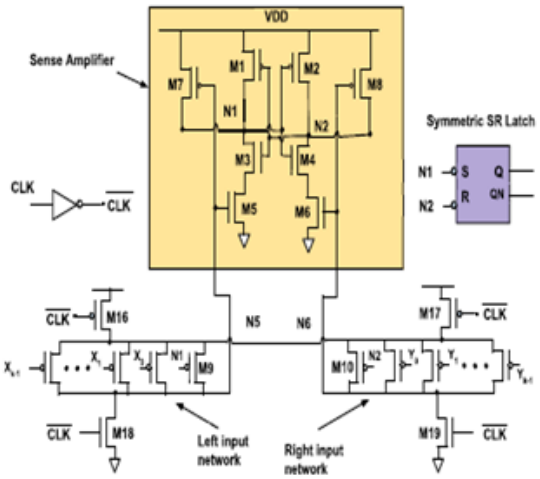
2. LITERATURE SURVEY

SENSE AMPLIFIER:

In modern computer memory, a sense amplifier is one of the elements which make up the circuitry on a semiconductor memory chip (integrated circuit); the term itself dates back to the era of magnetic core memory. sense amplifier is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a bit line that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory. Modern sense-amplifier circuits consist of two to six (usually four) transistors, while early sense amplifiers for core memory sometimes contained as many as 13 transistors. There is one sense amplifier for each column of memory cells, so there are usually hundreds or thousands of identical sense amplifiers on a modern memory chip. As such, sense amplifiers are one of the only analog circuits in a computer's memory subsystem.

3. CIRCUIT DESIGN

A.PNAND CELL:



Cell Operation

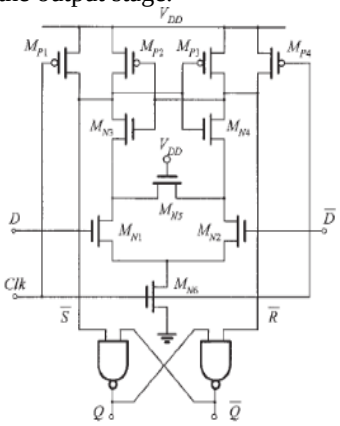
Fig. 1 shows the schematic of the threshold gate with k inputs, henceforth, referred to as pNAND-k. It consists of three main

components: 1) two groups of parallel pFET transistors referred to as the left input network (LIN) and the right input network (RIN); 2) a sense amplifier (SA),which consists of a pair of cross-coupled NAND gates; and 3) a set–reset (SR) latch. The cell is operated in two phases: reset (CLK = 0) and evaluation (CLK 0 → 1). For the moment, ignore the transistors M9 and M10 in the LIN and the RIN.1) Reset Phase: With CLK = 0, the two discharge devicesM18 and M19 pull nodes N5 and N6 low, which turn OFFM5 and M6, disconnecting all paths from N1 and N2 to ground. In addition, M7 and M8 are active, which results inN1 and N2 being pulled high. The n FETs M3 and M4 are ON. With N1 and N2 being high, the state of the SR latch does not change.

2) Evaluation Phase: This corresponds to when CLK 0 → 1. An input that results in active devices in the LIN and r active devices in the RIN is denoted by the signal assignment procedure will ensure that r. As a result, the conductance of the LIN is higher than that of the RIN. As the discharge devices M18 and M19 are turned OFF, both N5 and N6 will rise to 1. Due to the higher conductivity of the LIN, node N5 will start to rise first, which turns ON M5. With M3 = 1, N1 will start to discharge through M3 and M5. The delay in the start time for charging N6 due to the lower conductance of the RIN allows for N1 to turn ON M2 and turn OFF M4. Thus, even if N2 starts to discharge, its further discharge is impeded as M2 turns ON, resulting in N2 getting pulled back to 1. As a result, the output node N1 is 0 and N2 is 1. As the circuit and its operation are symmetric, if r, then the evaluation will result in N1 = 1 and N2 = 0. The active low SR latch stores the signals N1 and N2. During reset, when (N1, N2) = 1, the SR latch retains its state. After evaluation, if (N1, N2) = (0, 1), the output Q = 0, and if (N1, N2) = (1, 0), Q = 1, providing a dual-rail output for the threshold function being computed. Therefore, once evaluated after the rising edge of the CLK, the output *Q* of the cell is stable for the remaining duration of the clock cycle. Hence, it operates like an ETFF that computes a threshold function.

B.NOVEL SENSE AMPLIFIER-BASED FLIP-FLOP:

The main of the SAFF proposed in and is the slave element, composed by a set/reset (SR) NAND latch. While this circuit requires a minimum transistor number, it results in asymmetrical delays with a slow high-to-low clock-to-output delay. The performance gain is paid with an increased number of transistors in the output stage.



Timing elements, latches and flip-flops, are critical to performance of digital systems, due to tighter timing constraints and low power requirements. Short setup and hold times are essential, but often overlooked. Recently reported flip-flop structures achieved small delay between the latest point of data arrival and output transition. Typical representatives of these structures are sense amplifier-based flip-flop (SAFF), hybrid latch - flip-flop (HLFF) and semi-dynamic flip-flop (SDFF) .Hybrid flip-flops outperform reported sense-amplifier-based designs, because the later are limited by the output latch implementation. SAFF consists of the sense amplifier in the first stage and the R-S latch in the second stage,. The first stage of this flip-flop is the sense amplifier. It senses the true and complementary differential inputs. The sense amplifier stage produces monotonous transitions from high to low logic level on one of the outputs, following the leading clock edge. The S-R latch captures each transition and holds the state until the next leading clock edge arrives. Therefore, the whole structure acts as a flip-flop. The S-R latch operates as follows. Input S is a set input and R is a reset input. The low level at both S and R node is not permitted, guaranteed by the sense-amplifier stage. The low level at S sets the Q output to high, which in turn forces Q to low. Conversely, the low-level at R sets the Q high, which in turn forces Q to low. Therefore, one of the output signals is always delayed with respect to the other. The rising edge always occurs first, after one gate delay, and the falling edge occurs after two gate delays. This limits the performance of the SAFF. The S-R latch operates as follows. Input S is a set input and R is a reset input. The low level at both S and R node is not permitted, guaranteed by the sense-amplifier stage. The low level at S sets the Q output to high, which in turn forces Q to low. Conversely, the low-level at R sets the Q high, which in turn forces Q to low. Therefore, one of the output signals is always delayed with respect to the other. The rising edge always occurs first, after one gate delay, and the falling edge occurs after two gate delays. This limits the performance of the SAFF The output stage takes advantage of two possible logic representations for the output Q: Q=S+RQ´ and Q=R•(S+Q´), to produce four topologically equivalent pull-up and pull-down transistor networks. Given that the output stage is symmetric with respect to pull-up and pull-down circuits for Q and Q, both pull-ups and pull-downs can be implemented using the same circuit topology, thus making the output stage symmetrical. The circuit topology has only one transistor in each branch active in changing state, allowing smaller keeper transistors.

4. SIMULATIONS AND RESULTS

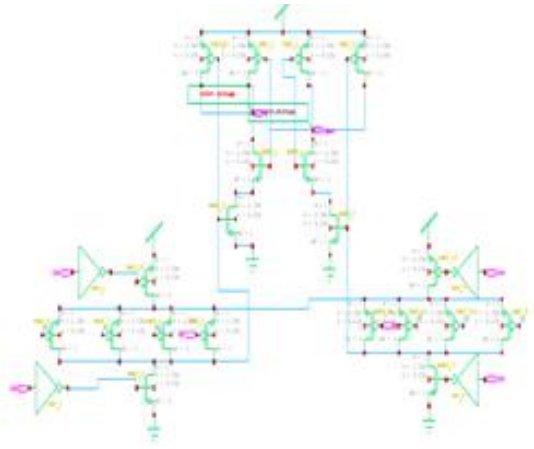


Figure.1. Schematic Pnand Cell

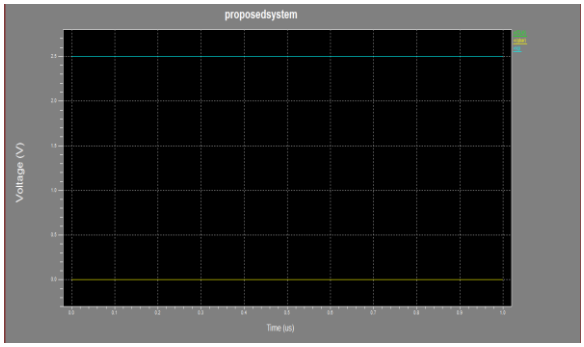


Figure.2. Waveform pNAND Cell

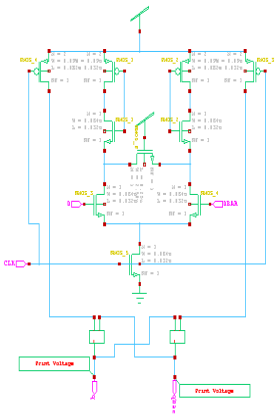


Figure.3. Schematic novel sense amplifier-Based Flip-Flop

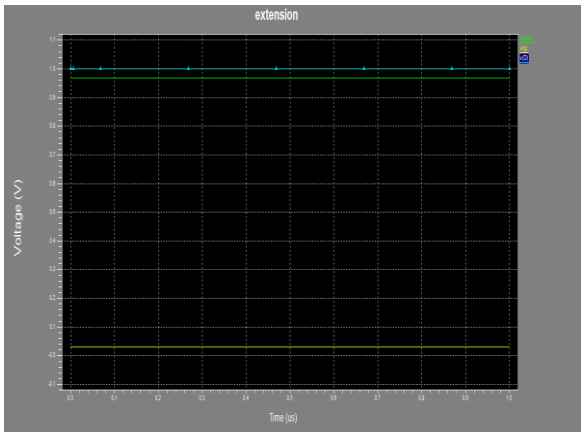


Figure.4. Wave form novel sense-Amplifier-Based Flip-Flop

Table.1. Comparsion Between Proposed And Existing

CIRCUIT	POWER	DELAY	POWER DELAYPRODUCT(PDP)
PNAND CELL	2.075401E-003W	3.98E-07	8.26E-10
NOVEL SAFF(SENSE AMPFLIER BASED FLIPFLOP)	6.474204E-005W	5.11E-09	3.31E-13

5. CONCLUSION:

In this paper, we described a new, automated methodology for the design of digital ASIC circuits using a combination of conventional logic gates and threshold logic flip-flops. The result is hybrid network that includes conventional logic gates and threshold gates. The methodology described in this paper was exercised on a number of complex function blocks, and significant improvements in power, leakage, area, and power variation were demonstrated.

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