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A Review on Design of Sampling Rate Converter using Symmetric Technique

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Abstract:
Sampling is a very important phase of digital signal processing. Converting one sampling rate of a signal to another is called sampling rate conversion. According to requirement the sampling rate of signal may be increased or decreased. Interpolation is a technique to increase sampling rate and decimation is a technique to decrease sampling rate of a signal. Rational sampling rate converter with FIR filter are more desirable and also become more interested and applicable in image resizing, software radios, digital audio resampling and medical applications. The basic sampling rate converter has many challenges in terms of performance parameters and process parameter variations. In this paper different techniques of sampling rate conversion and their outcomes are discussed.

Keywords: Sampling, Interpolation, Decimation, Filter, Polyphase, Multirate.

I. INTRODUCTION

Sampling is a very important phase of digital signal processing. In today world the demands for digital products with programmability are growing day by day. Various industries like audio, video, and cellular industry rely heavily on digital technology. A great part of digital technology deals with digital signal processing. This aspect in engineering has gained increasing interest, especially with much of the world now turning to wireless technology. Sampling rates can be increased or decreased according to requirement. Interpolation is a technique to increase sampling rate and decimation is a technique to decrease sampling rate of a signal. The multirate techniques are used to convert the given sampling rate to desired sampling rate and are called multirate system. The basic building blocks of multirate system are interpolators and decimators. This technique is used in many applications like digital audio, communication systems, speech processing, radar systems, antenna systems etc. Sampling rate converter is used in many communication and signal processing applications where two signals or systems having different sampling rates need to be interconnected. For example, in digital audio, the different sampling rates used are 32 KHz for broadcasting, 44.1 kHz for compact disc and 48 kHz for audio tape. In digital video, the sampling rates for composite video signals are 14.318MHz and 17.73MHz for NTSC and PAL respectively. But the sampling rates for digital component of video signals are 11.5 MHz and 6.75 MHz for luminance and color difference signal.

1.1Need of sampling-rate conversion

In digital audio applications, a number of sample frequencies are in use for example 32 KHz is used for broadcasting, 44.1 kHz used for compact disc and 48 kHz for audio tape. So for an application to be running successful sampling rate converters are very needful. Certain situations in which the application of sample-rate conversion is very useful are listed below:

i) When two digital audio systems are linked together, the sample frequency of one of the two systems may have to be altered. However, only one master clock can issue the correct moment of sampling in a digital system, so this inevitably leads to synchronization problems. Due to the different standards used, the interconnection of two audio devices becomes very cumbersome. Here, the application of sample-rate conversion is desirable.

ii) Even when the two devices to be connected have equal sample frequencies, synchronization problems will occur due to a (very) small difference in sampling frequency. This is especially true for systems where a lot of digital sources have to be aligned to one sample frequency before they can be mixed or processed, like in digital audio mixers or in digital broadcast stations. Here, sample-rate conversion can be applied to (re)synchronize the different sources.

iii)Although digital audio links are normally not subject to loss of code information, they definitely introduce a loss of timing information (jitter), due to long transmission lines. When such a jittering signal is used as a clock source for the DAC section, the analog performance at the output can be seriously degraded. Here also, sample-rate conversion in combination with a digital PLL can be used for jitter removal.

1.2 Sampling Rate conversion designs: Decimation

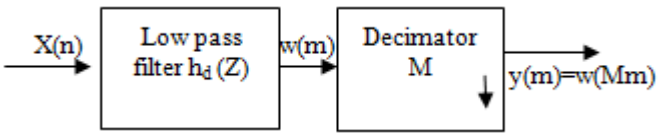

Figure. 1.1 Down sampler by factor of M

A reduction of sample rate (decimation) by a factor of *M* is achieved by sequentially discarding *M-1* samples and retaining every *M'th* sample. While discarding *M-1* of every *M* input samples reduces the original sample rate by a factor of *M*, it also causes input frequencies above one half the decimated sample rate to be aliased into the frequency band from DC to the decimated Nyquist frequency. To mitigate this effect, the input signal must be lowpass filtered to remove frequency components from portions of the output spectrum which are required to be alias free in subsequent signal processing steps.

A benefit of the decimation process is that the lowpass filter may be designed to operate at the decimated sample rate, rather than the faster input sample rate, by using a FIR filter structure.

Interpolation

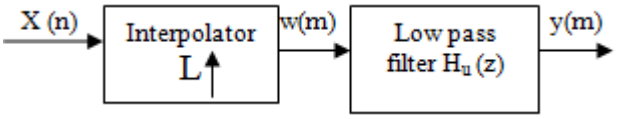

Figure. 1.2 Up sampler by factor of L

An increase in sample rate (interpolation) by a factor of *L* is achieved by inserting *L-1* uniformly spaced, zero value samples between each input sample. While adding *L-1* new samples between each input sample increases the sample rate by a factor of *L*, it also introduces images of the input spectrum into the interpolated output spectrum at frequencies between the original Nyquist frequency and the higher interpolated Nyquist frequency. To mitigate this effect, the interpolated signal must be lowpass filtered to remove any image frequencies which will disturb subsequent signal processing steps. A benefit of the interpolation process is that the lowpass filter may be designed to operate at the input sample rate, rather than the faster output sample rate, by using a FIR filter structure.

II. LITERATURE REVIEW

Yu Huijun in [1] has proposed novel design of sampling rate converter based on least square method. To improve the accuracy of signal resampling, a resampling realization method is proposed in this paper. It converts a resampling problem into a time-variable filter designing, so the least square method can be used to obtain the filter coefficients and obtain better accuracy. The experimental results proved that high accuracy signal resampling can be realized with the proposed method. There are two main ways to convert sample rate of a discrete time system. One is based on polynomial approximation Although that method has the advantage of high accuracy, the disadvantage is that it has high computation cost. Another is based on multi-rate techniques. This method has the advantage of low computing cost, but the disadvantage is that the filter designing is difficult. A new design of sample-rate converter based on least-square method is proposed to improve the resampling accuracy. To avoid the ill-conditioning problem which may arise in solving the least-square equations, QR decomposition based on householder transformation is used. This resampling method can obtain higher accuracy and easy be implemented. Robert Bregovic in [2] have proposed an efficient structure for implementing a linear-phase finite impulse response (FIR) filter of an arbitrary order N for the sampling-rate conversion by a rational factor of L/M, where L(M) is the integer up sampling (down sampling) factor to be performed before (after) the actual filter. In this implementation, the coefficient symmetry of the linear-phase filter is exploited as much as possible and the number of delay elements is kept as low as possible while utilizing the following facts. When increasing (decreasing) the sampling rate by a factor of L(M) , only every L_{th} input sample has a nonzero value (only every M_{th} output sample has to be evaluated). In this way, the number of required multiplications per output sample is reduced approximately by a factor of two compared with the conventional polyphase implementation. Oscar Gustafsson in [3] have shown that rational sampling rate conversion based on an FIR filter can be written as a constant matrix multiplication. It was shown that the proposed method in general reduces the arithmetic complexity of the realizations compared with using separate MCM blocks. Furthermore, it was shown that the number of registers varies between direct form and transposed direct form FIR filter based rational sample rate converters. The structure with the smallest number of registers depends on if the total sample rate is increased or decreased. It is shown that polyphase decomposed FIR filters for rational sampling rate conversion can be viewed as a matrix multiplication and several parallel delay chains. The delay chains are placed before or after the matrix multiplication depending on whether direct form or transposed direct form subfilters are used. Eleftherios Fysikopoulos in [4] have proposed and evaluate a simple, open source, data acquisition (DAQ) tool, which provides accurate results for nuclear imaging applications. For this purpose a Xilinx Spartan3E Starter Kit, which is one of the simplest Field Programmable Gate Arrays (FPGA) evaluation boards, was used. Results have shown that the FPGA based data acquisition system i) provides accurate digitization of the PSPMTs anode signals in various conditions and ii) gives similar energy spectra when SiPMs are used. Experimental evaluation has shown that it provides accurate results, comparable to those obtained by standard NIM electronics in three different experimental setups. Spatial and energy resolution values were satisfactory, taking into consideration the limitations of the board. A. J. N. Batista in [5] have presented that eight independent multi-rate signal interpolators, with real-time change of rate capability, were implemented on a field programmable gate array. The interpolator main building blocks are a cascaded integrator-comb (CIC) filter and the respective compensation filter. The latter performs a fixed rate change of 4 and was implemented as a 129 taps finite impulse response (FIR) filter. The FIR filter coefficients were attained from the MATLAB simulation, based on the inverse sinc(x) function. Each interpolator over-samples the multiple data rate digital signals stored at the Joint European Torus (JET) pulse database to a fixed sampling rate of 40 MSPS. These signals are subsequently converted to the analog domain by 16 bit digital-to-analog converters to be used as stimulus for testing real-time control tools and systems at JET. N. Aikawa in [6] presents a kernel with block structure for sampling rate conversion. The kernel proposed has the block structure that the impulse response of the sampling section since the third is represented by the polynomial used for the second sampling section. Therefore, the filter has less memory. As the filter proposed has the impulse response approximated by polynomials, it is unnecessary to redesign whenever the sampling rate is changed. Moreover, the filter has the advantage that it is possible to correspond to arbitrary fractional sampling rate conversion. Robert Bregovic in [7] have presented that by designing frequency-response masking approach filters building the FB in such a way that the periodic filters are evaluated at the input sampling rate and the masking filters at the output sampling rate, the design as well as the implementation complexity can be further reduced when compared with the designs obtained by using other existing techniques.

Takahashi N in [8] have presented a digital audio processing application , there are multiple standard sampling rates, for example, 48kHz for studio work, 44.1kHz for compact disk(CD) mastering. Therefore, sampling rate conversion is needed to interchange signals from one field to another. A rational sampling rate conversion by L/M can be done cascading an L-fold up-sampler and an M-fold down-sampler with a linear phase FIR lowpass filter in the middle. When

both L and M have large values, the lowpass filters are required to have an extremely narrow normalized bandwidth and a sharp transition characteristic, causing difficulty in design and implementation. This paper describes a technique to overcome this difficulty for the case both L and M are composite numbers, giving an multistage converter structure where each stage is consisting of an up-sampler and a down-sampler, both of a small conversion ratios, with a filter having not so sharp normalized transition characteristic in the middle, remarkably reduced total computation complexity. Haipeng Kuang in [9] presented A novel 8-channel, area-efficient, low-power audio sampling rate converter is proposed in this paper, conversion ratio is 2:1 and 4:1. Filter design and implementation are the key points for the converter. First, excluded data and coefficients memories, adopting multiplier-free arithmetic unit (AU) and rounding methods allows its realization in a cell area of only 0.038 mm^2 in 0.18 mum technology; next a new timing division multiplexer (TMD) scheme lowers clock working rate to minimum in order to save power; third, a novel memory addressing scheme reduces 20% data memory at least. Experiments show proposed methods could not only saved hardware resources but also reduce power consumption, so it is very suitable for consumer electronics. Raini J in [10] presented data receivers for storage systems normally operate at a fixed sampling rate $1/T_S$ that is asynchronous to the baud rate 1/T.

A sampling rate converter (SRC) serves to convert the incoming signal from the asynchronous to the synchronous clock domain. These receivers also contain an equalizer that serves to suppress inter symbol interference and noise. To limit receiver complexity, equalization burden can be shifted towards the SRC. This possibility is not exploited in any existing SRC. This paper presents SRC design methods that combine group delay flatness and out-of-band rejection criteria with the minimum mean square error equalization criterion. Numerical examples for an idealized optical recording channel validate the design methods. Varma in [11] presented a multiband signal, the minimum sampling rate required for an arbitrary sampling method, which allows perfect recons truction, is NB, where N is the number of bands and B is the maximum bandwidth. It has been proposed in the literature that, if the carrier frequency information of a multiband signal is not known a priori, then we require a minimum sampling rate of 2NB for perfect reconstruction. Modulated wideband converter (MWC)is a recently introduced blind sampling method.

Unlike the traditional sampling methods, where the continuous-time signal can be expressed in terms of samples using simple Whittaker-Shannon interpolation, there is no closed-form expression relating the samples generated by MWC and the continuous-time signal. In order to reconstruct the signal, we require compressive sensing (CS) algorithm. The CS algorithm, simultaneous orthogonal matching pursuit (SOMP) used in the reconstruction stage requires a minimum rate of 4N B log (M/2N), which is nearly twice the theoretical rate. In this paper, we propose a new greedy algorithm, which exploits the clustered sparse structure of the multiband signals to sample at near-theoretical rates.

III. CONCLUSION

From the literature survey it can be concluded that various approaches of sampling rate converter designed by using various different techniques has presented and unified into an integrated design methodology. Some techniques give good results but complexity increases. In most of the research work two main ways are used to convert sample rate of discrete time system (1) Polynomial approximation (2) Multirate techniques. Polynomial approximation has advantage of high accuracy but disadvantage is that it has high computation cost. In multirate, various techniques have been applied in order to reduce the implementation complexity of overall system i.e. polyphase structure is derived for efficiently implementing the filter, a fast fourier transform based cyclic algorithm has been used. Further, various structures introduced different delays to the signal. In all of the aforementioned approaches, the coefficient symmetry has not been used. Neither of those methods could achieve a reduction in the multipliers and adders. Achieving such a reduction is the goal of this research.

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