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Design and Implementation of Sampling Rate Converter Using Symmetric Technique

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Abstract:
Sampling rate conversion is a process used to convert sampling rate of a signal from one rate to another. Interpolation and decimation are operations used respectively to increase and reduce the sampling rate or frequency, usually by an integer factor. In this paper we designed an efficient sampling rate conversion structure for higher engineering applications by a factor of L/M, where L is up-sampling factor and M is down-sampling factor. In the proposed designed, the number of required multiplications and adder per output sample is reduced. For implementation we use linear phase FIR filter. The symmetric FIR filter has shown reduction in multipliers and adders.

Keywords: Multi-rate system, Poly-phase, FIR filter, Interpolation, Decimation.

I. INTRODUCTION

Sampling rate conversion is a process used to convert sampling rate of a signal from one rate to another. Interpolation and decimation are operations used respectively to increase and reduce the sampling rate or frequency, usually by an integer factor. Increasing of a sampling rate requires that new values, not presented in the signal, be computed and inserted between the existing samples. The new value is estimated from a neighbourhood of the samples of the original signal. Similarly, in decimation a new value is calculated from a neighbourhood of samples and replaces these values in the lower sampling rate. Integer factor interpolation and decimation algorithms may be implemented using efficient Finite Impulse Response (FIR) filters and are therefore relatively easy to implement. This technique is used in many applications like digital audio, communication systems, speech processing, radar systems, antenna systems etc. Sampling rates can be increased or decreased according to requirement. Increasing the sampling rate known as interpolation and decreasing the sampling rate is decimation. The multi-rate techniques are used to convert the given sampling rate to desired sampling rate and are called multi-rate system. The basic blocks of multi-rate system are interpolators and decimator. Combination of these blocks represent a system in which sampling rate is changed by a rational factor L/M. The block diagram of rational sampling rate converter is as follows:

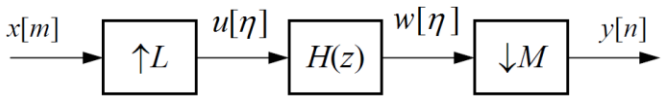


Figure .1. Sampling Rate Converter.

Figure 1 shows that the input signal is up-sampled by factor of L, after that signal is filtered by transfer function H(Z), and resulting signal is down-sampled by a factor of M. A filter is used in between decimation and interpolation to suppress aliasing and to remove imaging respectively [2]. The relation between input sampling rate f_{in} and output sampling rate f_{out} is given by

$$f_{out} = \left(\frac{L}{M}\right) f_{in} \qquad (1)$$

$$H(z) = \sum_{k=0}^{N} h_k z^{-k} \qquad (2)$$

Where

$$h_{N-k} = h_k \qquad k = 0,1,...,N \qquad (3)$$

H(z) is transfer function of linear phase FIR filter.
Most of the cases, linear phase FIR filters are used. They are better than IIR filters because they have no feedback loops and can be implemented in a multi-rate system easily.

1.1 Decimation

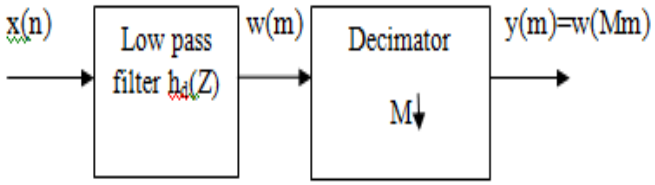


Figure.2. Down-Sampler by a factor of M

A reduction of sample rate (decimation) by a factor of *M* is achieved by sequentially discarding *M-1* samples and retaining every *M'th* sample. While discarding *M-1* of every *M* input samples reduces the original sample rate by a factor of *M*, it also causes input frequencies above one half the decimated sample rate to be aliased into the frequency band from DC to the decimated Nyquist frequency. To mitigate this effect, the input signal must be lowpass filtered to remove frequency components from portions of the output spectrum which are required to be alias free in subsequent signal processing steps. A benefit of the decimation process is that the lowpass filter may be designed to operate at the decimated sample rate, rather than the faster input sample rate, by using a FIR filter structure.

1.2 Interpolation

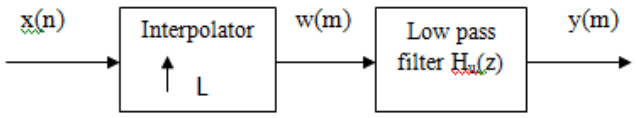


Figure. 3. Up-Sampler by a factor of L

An increase in sample rate (interpolation) by a factor of *L* is achieved by inserting *L-1* uniformly spaced, zero value samples between each input sample. While adding *L-1* new samples between each input sample increases the sample rate by a factor of *L*, it also introduces images of the input spectrum into the interpolated output spectrum at frequencies between the original Nyquist frequency and the higher interpolated Nyquist frequency. To mitigate this effect, the interpolated signal must be lowpass filtered to remove any image frequencies which will disturb subsequent signal processing steps. A benefit of the interpolation process is that the lowpass filter may be designed to operate at the input sample rate, rather than the faster output sample rate, by using a FIR filter structure.

1.3 Need of sampling-rate conversion

There are three important situations in which the application of sample-rate conversion is very useful. They are listed below:
i) When two digital audio systems are linked together, the sample frequency of one of the two systems may have to be altered. However, only one master clock can issue the correct moment of sampling in a digital system, so this inevitably leads to synchronization problems. Due to the different standards, the interconnection of two audio devices becomes very cumbersome.
ii) Even when the two devices to be connected have equal sample frequencies, synchronization problems will occur due to a (very) small difference in sampling frequency. This is especially true for systems where a lot of digital sources have to be aligned to one sample frequency before they can be mixed or processed, like in digital audio mixers or in digital broadcast stations.
iii)Although digital audio links are normally not subject to loss of code information, they definitely introduce a loss of timing information (jitter), due to long transmission lines. When such a jittering signal is used as a clock source for the DAC section, the analog performance at the output can be seriously degraded.

1.4 Poly-phase Implementation

The basic procedure of re-sampling a discrete time sequence by an integer factor consists of either inserting a sequence of zero samples between each input sample followed by low pass anti-imaging digital filter or low pass anti-aliasing filtering of an input signal and discarding some samples at the output. To improve the computational complexity of digital filter, poly-phase filters were introduced. Using this implementation at interpolator the multiply by zero samples can be eliminated and at decimator low pass filter output computation are avoided which are to be discarded at the output [12]. The realization of higher order FIR filter in parallel structure can be done based poly-phase decomposition. The transfer function of digital FIR filter is to be decomposed into M or L lower order transfer function called poly-phase components which are added together later on to form the original over all transfer function. An FIR digital filer can be implemented as a parallel structure of M or L poly-phase components, which are added together at the output. The poly-phase component is usually implemented in the direct transversal for Figure 3.7 shows a decimator composed of series connections of an FIR filter implemented as a parallel connection of M poly-phase branches and factor of M down sampler. In figure 3.8 bobble indentifies describe in section 3.2 are used to reduce the computational complexity SRC. Similar structure for interpolation can be implemented as shown in figure 3.8

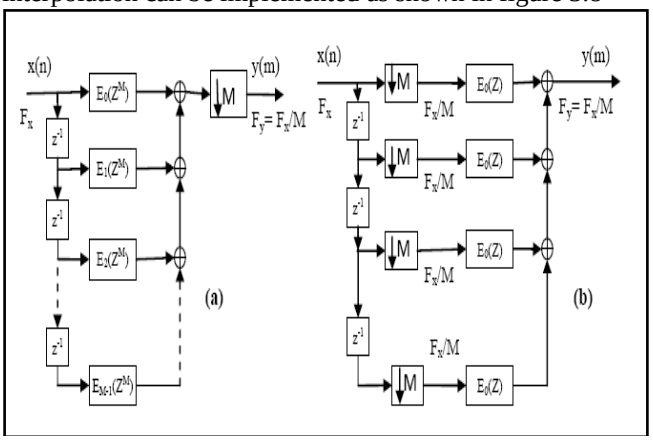


Figure .4. Polyphase implementation of Decimator (a) Poly-phase structure followed by decimator (b) Computational efficient structure of decimator

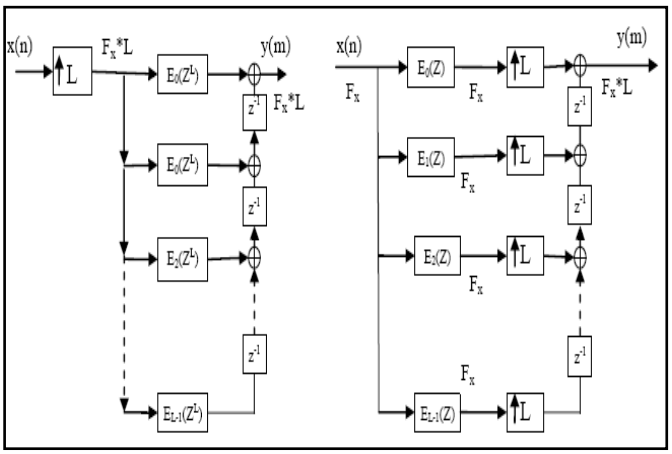


Figure.5. Poly-phase implementation of Interpolator (a) Poly-phase filter structure preceded by Interpolator (b) Computational efficient structure of Interpolation

1.5 Advantages of FIR filter over IIR in multirate systems

Most FIRs are linear-phase filters; when a linear-phase filter is desired, a FIR is usually used. Linear Phase refers to the condition where the phase response of the filter is a linear (straight-line) function of frequency (excluding phase wraps at +/- 180 degrees). This results in the *delay* through the filter being the same at all frequencies. Therefore, the filter does not cause "phase distortion" or "delay distortion". The lack of phase/delay distortion can be a critical advantage of FIR filters over IIR and analog filters in certain systems, for example, in digital data modems. FIR filters are usually designed to be linear-phase (but they don't have to be.) A FIR filter is linear-phase if (and only if) its coefficients are symmetrical around the center coefficient, that is, the first coefficient is the same as the last; the second is the same as the next-to-last, etc. (A linear-phase FIR filter having an odd number of coefficients will have a single coefficient in the center which has no mate.) Because only a fraction of the calculations that would be required to implement a decimating or interpolating FIR in a literal way actually needs to be done. In contrast, since IIR filters use feedback, every input must be used, and every input must be calculated because all inputs and outputs contribute to the feedback in the filter.

II. RATIONAL SAMPLING RATE CONVERTER

This section shows, some relations for system in Fig 1. These relations are used in section 3 and 4 for generating an implementation structure for rational sampling rate converter. There are two parts in this section. First, time domain input output relation and second is compact matrix representation of input output relation. Matrix representation is more suitable to generate an efficient implementation [2].

Basic input output relations between input and output samples

For sampling rate converter shown in Fig 1, the time domain relations are given as

$$u[n]=\begin{cases} x\left[\frac{n}{L}\right] & for\ n=0,L,2L,... \\ 0 & otherwise \end{cases} \quad (1)$$

$$w[n]=\sum_{k=0}^{N} h_k u[n-k] \quad (2)$$

$$y[n]=w[Mn] \quad (3)$$

Rational Sampling Rate Conversion factor 2/3

Based on the discussion in Chapter-1 we will design rational sampling rate converter with L=2, M=3, and N=11. In this case output sampling frequency is decreased by 3/2 with respect to input sampling frequency. For this implementation we use matrix as given in chapter-1. Based on that matrix the relations between L=2 consecutive output samples, y[n] and y[n+1] and the input samples x[m] can be expressed as

$$\begin{bmatrix} y[n] \\ y[n+1] \end{bmatrix}=\begin{bmatrix} 0 & h_0 & h_2 & h_4 & h_6 & h_8 & h_{10} \\ h_1 & h_3 & h_5 & h_7 & h_9 & h_{11} & 0 \end{bmatrix}.x_{m+1,m-5} \quad (4)$$

Where $x_{m+1,m-5}$ is defined by equation

After utilizing coefficient symmetry given by (), above equation can be rewritten as

$$\begin{bmatrix} y[n] \\ y[n+1] \end{bmatrix}=\begin{bmatrix} 0 & h_0 & h_2 & h_4 & h_5 & h_3 & h_1 \\ h_1 & h_3 & h_5 & h_4 & h_2 & h_0 & 0 \end{bmatrix}.x_{m+1,m-5} \quad (5)$$

In order to generate a form that is appropriate for an efficient implementation, above equation is decomposed into two distinct parts as follows

$$\begin{bmatrix} y[n] \\ y[n+1] \end{bmatrix}=h_4x[m-2]\begin{bmatrix}1\\1\end{bmatrix}+h_1x[m-5]\begin{bmatrix}1\\0\end{bmatrix}+h_1x[m+1]\begin{bmatrix}0\\1\end{bmatrix}+\begin{bmatrix} h_0 & h_2 & h_5 & h_3 \\ h_3 & h_5 & h_2 & h_0 \end{bmatrix}\begin{bmatrix} x_{m,m-1} \\ x_{m-3,m-4} \end{bmatrix} \quad (6)$$

Three terms are very simple and can be implemented directly. Filter coefficient matrix in the forth term is called Centro symmetric matrix. And can be implemented by using following decomposition.

$$\begin{bmatrix} h_0 & h_2 & h_5 & h_3 \\ h_3 & h_5 & h_2 & h_0 \end{bmatrix}\begin{bmatrix} x_{m,m-1} \\ x_{m-3,m} \end{bmatrix}=\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}\begin{bmatrix} c_1 & c_2 & 0 & 0 \\ 0 & 0 & d_2 & d_1 \end{bmatrix}x^{(2)}_{m,m-4} \quad (7)$$

Where

$$c_1=(h_0+h_3)/2$$
$$c_2=(h_2+h_5)/2$$
$$d_1=(h_0-h_3)/2$$
$$d_2=(h_2-h_5)/2$$

$$x^{(2)}_{m,m-4}=\begin{bmatrix} I_2 & J_2 \\ J_2 & -I_2 \end{bmatrix}\begin{bmatrix} x_{m,m-1} \\ x_{m-3,m-4} \end{bmatrix} \quad (8)$$

Variables c_1, c_2,d_1 and d_2 depend only on the filter coefficients and can be pre calculated. The matrices I_2 and J_2 are 2 by 2 identity and counter identity matrices, respectively. The implementation structure for sampling factor 2/3 is shown in fig.

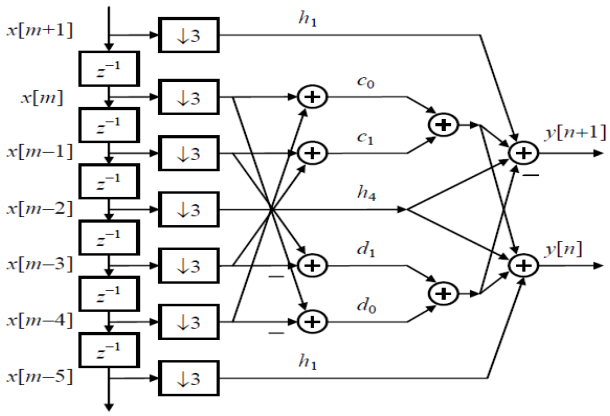


Figure .6. Implementation Structure for Rational Sampling Rate Converter

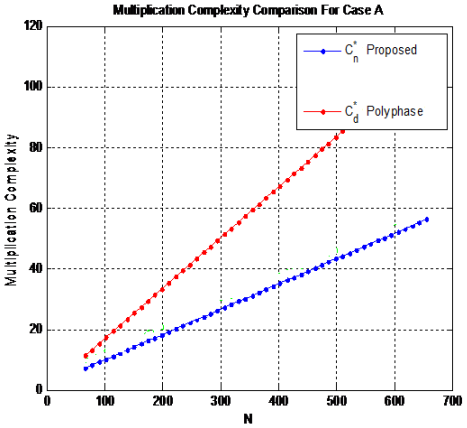
For generating y[n] and y[n+1], this structure requires 7 multiplications and 12 additions. This means it requires 3.5 multiplications and 6 additions per output sample. Same system without utilizing the coefficient symmetry, requires 6 multiplications and 5 additions per output sample.

III RESULTS AND DISCUSSIONS

This section shows that how proposed method is better than existing ones. As seen in figure 3, the proposed method gives results having low implementation complexity as compare to polyphase implementation. Results show that when the filter order is increased then complexity is decreased.

Table.1.Implementation Complexity of Sampling Rate Converter

	Proposed	
N	**Cn***	**Cn+**
211	19.16	23.667
214	19.167	23.667
23	3.167	2.333
209	18.667	23.00
210	19.167	23.667
212	19.167	23.667



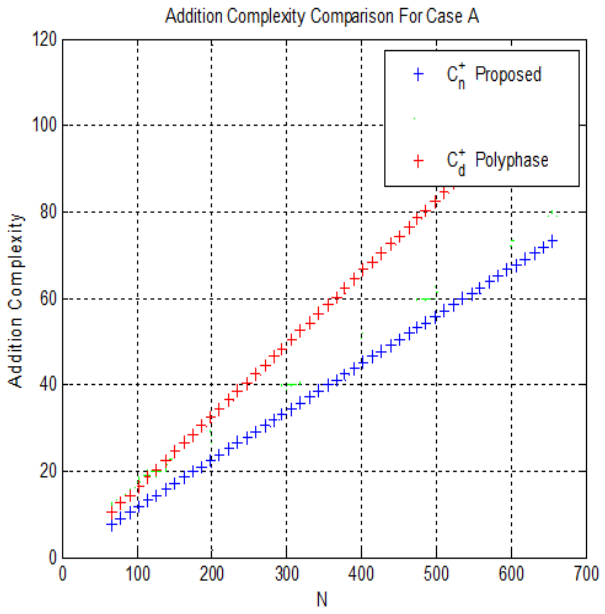


Figure .7. Implementation complexity for rational sampling rate converters by 6/11. (a) Number of multiplications(c*) per output sample. (b) Number of additions(c+) per output sample.

IV. CONCLUSION AND FUTURE WORK

In this paper an efficient structure is designed for sampling rate converter having rational factor L/M. The proposed implementation shows reduced number of multiplications per output sample as compare to polyphase implementation. Finally the implementation complexity of proposed approach is evaluated and with the help of some examples, efficiency of the proposed implementation is compared with others. In sampling rate conversion system computational complexity can further be reduced by many other efficient implementations such as farrow filtering structure. Efficient implementation using Lth band can be applied at each stage of multistage structure defined in thesis to further reduce the computational complexity

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