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Design of Sequential Circuits with Timing Analysis and Considerations

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Abstract:
Digital design techniques play a major role in VLSI designing. Growth in the complexity of circuits and performance requirements has necessitated the use of computer aided design tools. Our goal is to analyse the designing of sequential circuits to understand the timing considerations of various circuits for analysing the hazards & races encountered in them.

Keywords: sequential, setup time, propagation delay

I. INTRODUCTION

Digital electronics is classified into combinational logic and sequential logic. Combinational logic output depends on the inputs levels, where the outputs are entirely dependent on the current inputs. Although every digital system is likely to have combinational circuits, most systems encountered in practice also include storage elements, which result into another category of circuits, commonly known as sequential circuits. Unlike the combinational circuits, sequential logic output depends also on stored levels along with the input levels. the outputs in a sequential circuit are not only a function of the inputs, but also of the present stage of the storage elements. The next stage of the storage elements is also a function of external inputs and the present state. Thus, a sequential circuit is specified by a time sequence of inputs, outputs and internal states. There are basically two main types of sequential circuits. Their classification depends on the timing of their signals. These are

- Synchronous Sequential Circuits
- Asynchronous Sequential Circuits

In synchronous sequential circuits, the change of internal state occurs in response to synchronized clock pulses. On the other hand, asynchronous circuits do not use clock pulses. The memory elements used in sequential circuits are basically of following two types. These are:

- Clocked Flip Flops
- Unclocked Flip Flops or Time-delay elements

II. TIMING PARAMETERS AND METRICES

Like combinational circuits, when sequential circuits, such as edge-triggered flip-flops, are physically implemented, they exhibit certain timing characteristics. Unlike combinational circuits, these characteristics are specified in relation to the clock input. Since flip-flops only change value in response to a change in the clock value, timing parameters can be specified in relation to the rising (for positive edge-triggered) or falling (for negative-edge triggered) clock edge. The following parameters specify sequential circuit behaviour. Unless otherwise specified, the following descriptions pertain to positive edge-triggered circuits. Similar definitions can be made for negative edge-triggered circuits.

• **Propagation delay (tClk-Q)** -This value indicates the amount of time needed for change in the flip flop-clock input (e.g. rising edge) to result in a permanent change at the flip-flop output (Q). When the clock edge arrives, the D input value is transferred to output Q..
• **Contamination delay (tcd)** -This value indicates the amount of time needed for change in the flip-flop clock input to result in the initial change at the flip-flop output (Q)..
• **Setup time (ts)** -This value indicates the amount of time before the clock edge that data
input D must be stable.
• **Hold time (th)** -This value indicates the amount of time after the clock edge that data input D must be held stable.

III. GATE DELAYS

Transistors within a gate take a finite amount of of time to switch. This means that a change on the input of a gate takes a finite amount of time to Signal rise time Signal fall time cause a change on the output. This time is known as **Propagation Delay**. Smaller transistors mean faster switching times. A Semiconductor companies are continually finding L new ways to make transistors smaller, which means transistors are faster, and more can fit on a die in H the same area.

Tplh --time between a change in an input and a low to high change on the output. Measured from 50% point on input signal to 50% point on the output signal. The 'lh' part (low to high) refers to H OUTPUT change, NOT input change.

Tphl --time between a change in an input and a L high to low change on the output. Measured from tplh tphl 50% point on input signal to 50% point on the output signal. The 'hl' part (high to low) refers to OUTPUT change, NOT input change.

IV. DESIGN AND WAVEFORM

We are using two different designs of T-Flip Flop circuit for studying effects of design on timing parameters.

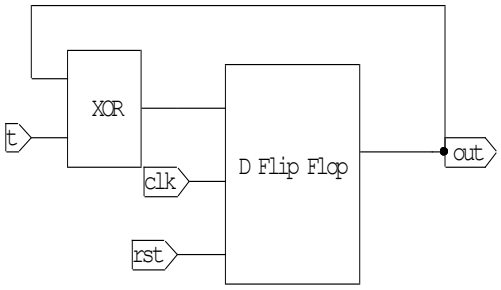

Figure.1. Design 1

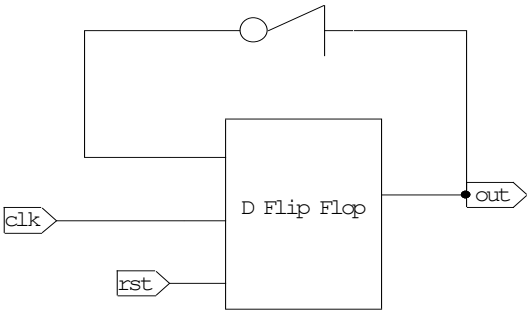

Figure.2. Design 2

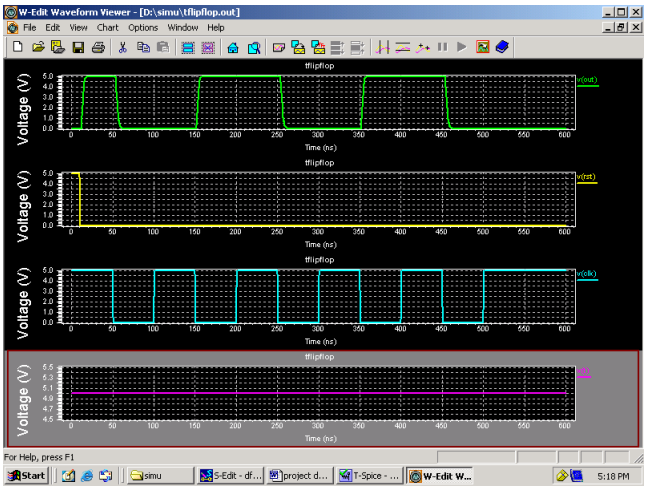

Figure.3. Waveform for design 1

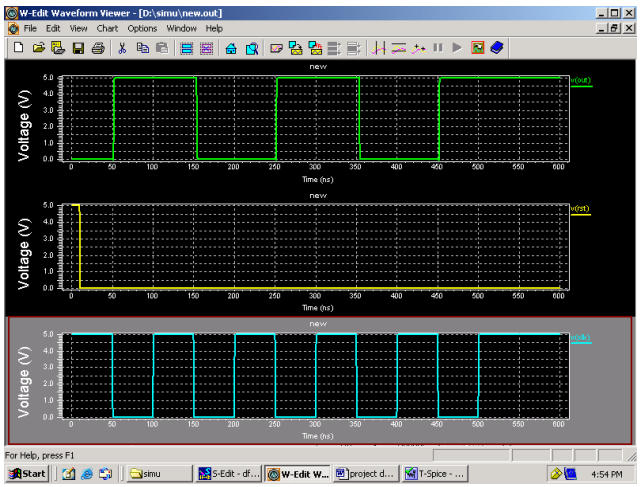

Figure.4. Waveform for design 2

V. TIMING ANALYSIS

DESIGN 1: PROPAGATION DELAY

High to Low =50% o/p – 50% clock
= 255.80ns – 250.47ns
= 5.33ns

Low to High =50% o/p – 50% clock
= 153.76ns – 150.49ns
= 3.27ns

DESIGN 2: PROPAGATION DELAY

High to Low =50% o/p – 50% clock
= 52.08ns – 50.50ns
= 1.52ns

Low to High =50% o/p – 50% clock
= 154.19ns – 150.49ns
= 3.70ns

VI. CONCLUSION

As can be seen from the timing values, the T flip flop designed using inverter gives lesser propagation delays than the one that was designed using an XOR gate. Sequential circuits are such a vast topic that any length of analysis done for these circuits will always be insufficient. We tried to study and analyze the synchronous and asynchronous circuits along with their timing considerations .However; we could only calculate the set up and hold time as well as the propagation delays for these circuits.

VII. REFERENCES

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