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Review of Leakage Power Reduction Technique in CMOS Circuit using DSM Technology

Anjali Sharma[1], Jyoti Jain[2]
M. Tech Scholar[1], Professor[2]
Department of Electronics and Communication
Sagar Institute of Research and Technology, Bhopal, India

Abstract:
The rapid growth of portable devices with enhanced computational capabilities and wireless communication has resulted in high power dissipation and heating. These portable devices require ultra low power consumption because of their limited battery capabilities. Previously, it was a challenge for VLSI designers to have high performance with minimal size. In sub-nanometer design leakage in static power is exceeding dynamic power consumptions. The performance of the chip is maintained by high driving capabilities at lower supply voltage, thus VTH is reduced and hence the performance of the chip is maintained. However reduction in the value of Threshold Voltage (VTH) results a exponential increase in the value of ISUB as VTH is directly proportional to Subthreshold Leakage Current (ISUB). In modern electronic devices power consumption is major design issue and is necessary to have a suitable power management in the design of circuits where standby modes and switching is responsible for the performance of the system. In this survey we try to use modest technique for leakage power consumption by all the conventional gates and study various leakage reduction techniques over various gates at 32nm and 45nm process technology using supply voltage of 0.9V and 0.8V HSPICE simulator at100MHz frequency.

Keywords: Low Power Consumption Design, Leakage power reduction, Integrated Circuits, Very Large Scale Integration.

1. INTRODUCTION

In a digital Complementary Metal Oxide Semiconductor transistor circuits dynamic power dissipation is major concern in total power consumption. Approach used for efficient dynamic power reduction is done by reducing the supply voltage. But as the supply voltage is reduced the circuit performance is degraded [4].So, for maintaining the circuit performance with the reduction in the supply voltage there should also be reduction in the threshold voltage. Battery life is directly effected in case of lower size transistor as they leak more power through the source in the idle state of the electronic devices [5]. As, enhancement in the field of electronics is done customer needs have changed and they demand portable devices as efficient as the non portable devices, it is seen that battery requirements have changed and there is a need for higher battery capacity. So, it is necessary for the designers to switch to a technology of low power CMOS Very scale integration design so that the supply voltage of the IC is reduced which results in the reduction of switching power dissipation in micron level devices which is responsible for the major power consumption[2]. Subthreshold leakage power dissipation is becoming more dominating among all leakage sources of the device below 90nmtechnology. The leakage power contribution can result in the power dissipation of up to 42% in the power dissipation of a CMOS VLSI design circuit in 90nm technology[12].Here, in this work we try to explore the cause of leakage in CMOS VLSI circuits and some of the gates of standard library are modified to reduce the leakage in the circuit in the standby mode with no major technology modification[9].Among all the leakage sources of device subthreshold leakage power dissipation is the most dominating below 90nm process technology. In this paper the leakage current is reducing in pull down network on the Circuit. Here in this technique we use a combination of PMOS in the pull down network. Scaling down of the technology has resulted in the increase of leakage current of transistor. Gate drain leakage, drain-induced barrier, weak inversion effect and gate-oxide tunneling lowering are major source of leakage current in the transistor. It is observed by deep sub- micron meter devices that gate leakage, threshold voltages, and low threshold voltages are the dominating source of leakage current. This effect can be increased by technology scaling. The GIDL (Gate induced drain leakage) and BTBT (base to base tunneling) also result in a significant effect on advanced CMOS VLSI devices [11]. The solution proposed should be considered for both at circuit level and process technology level in deep sub-micron meter CMOSVLSI circuits. This is a leakage reduction technique in run time which results in utilization of the substrate (body) terminal of the CMOS transistor to modify VTH of a transistor dynamically during operation of the circuit. The sum of electronic charges present in inversion layer and the negative ionic charge in the depletion region are balanced by positive charge on the gate. During RBB (Reverse Body Bias) of a MOSFET, the width of the depletion region beneath the gate increases difference between the source and body terminals Body to Source Voltage (VSB)[8]. The objective here is to reduce the leakage power consumption with the help of technology scaling using large number of gates per chip. So as to develop a technique for reduction of leakage which focuses on the stacking effect of transistor circuits using high dielectric (high–K)library to minimize Gate current IGATE. No Dependence of the technology variation, and taking the advantages of stacking effect. Extra supply voltage requirement is zero and additional controller like Reverse Body Bias technique. This also results in Solving in polynomial time (less complexity in time).Keeps trade-off between power, area and delay [2].

2. RELATED WORK: There are various approach used for the control of leakage current at transistor level in CMOS

design circuits [12]. INDEP (Input Dependent) approach [1] is the technique which mitigates the leakage current in nano scale CMOS circuits. This technique uses a combination of two extra transistors inserted between pull up and pull down network which are used in the input logic dependent. This technique is highly useful for static CMOS design circuits with sufficient delay penalty [20]. Here the guidelines are proposed in general terms so they can be utilized in form in any application or process technology.

The power consumption of a logic gate is given by:-

$$P_{avg\,gate} = P_{switching} + P_{shortcircuit} + P_{leakage} \qquad 1.1$$

Where $P_{switching}$ is the power consumed due to charging and discharging of the circuit capacitances and $P_{shortcircuit}$ is the power consumed due to the short circuit between V_{DD} and ground during output transitions and $P_{leakage}$ is leakage power consumption. Static (leakage) power ($P_{Leakage}$) is consumed by the circuit leakage current in its steady state i.e., When the circuit is "powered-on". Collectively, dynamic power and short circuit power are called switching power. Switching power dissipates when logic state of input signal Change in CMOS circuits.

Subthreshold leakage current (I_{sub} the subthreshold current flows due to three main reasons: Drain Induced Barrier Lowering (DIBL) effect, weak inversion effect and the direct punch-through of the electrons between drain and source. The DIBL effect occurs at higher drain voltages where threshold voltage of transistor reduces. Depletion region of the p-n junction between the drain and body increases with the increase in drain voltages which increases more under the gate voltage.

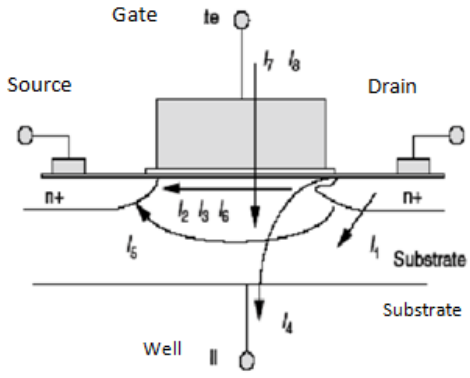

Figure.1.

The source injects carriers into the channel surface (independent of gate voltage).Narrow width of the transistor can also modulate the threshold voltage and the subthreshold current.

$$I_{sub} = \mu_0 . C_{ox} . \frac{W}{L} . V^2 . e^{1.8} . e^{\frac{(V_{gs} - V_T)}{nV}} \qquad (1.1)$$

Band to band tunnelling current While studying about reverse leakage current we came to know that within the geometry of the device, some junction Diodes are present. Because of the reverse biased diode a voltage is developed across the diode and high electric field Across this reverse biased p-n junction cause significant current known as Band to band tunneling current. This band To band tunneling current are larger than reverse biased leakage current in deep submicron technology.

Gate induced drain leakage current Gate induced drain leakage current occurs due to high electric
Field in the drain junction. This current occurs because of short channel length due to which a high electric field is created. Even a small voltage creates a large electric field.

Gate oxide tunnelling current Tunnelling through gate oxide occurs because thickness of Gate oxide layer is gradually reduced as technology is reducing [7]. The GIDL and BTBT (base to base tunneling) may also have a significant effect on advanced CMOS devices. The solution should be considered both at circuit level and process technology level in deep sub-micron meter CMOS circuits. At circuit level, variable threshold, dynamic threshold, dual threshold, multi-threshold and transistor stacking techniques can effectively reduce the leakage current in memory and high performance CMOS circuits. At the process technology level, halo doping and retrograde techniques are used to reduce leakage current. Such well engineering techniques also improve short-channel characteristics.

Gate current due to hot carrier injection Another kind of gate leakage is known as the gate current due to hot carrier injection. For a very small gate voltage because The smaller thickness of the Silicon dioxide layer electric field becomes so high that it creates electrons of very high energy known as hot electrons(hot carriers). Those hot electrons acquire a very high energy that they can pass through the Silicon dioxide layer.

2.1 Dual Threshold (Dual-VTH) Technique Dual-Threshold CMOS technique is frequently used at sub- system design level. For this technique a sub-system is implemented with low VTH transistors or a high VTH transistors depending upon whether they lie in the critical path or not [7-8]. Here, various algorithms are used to take decision regarding critical path of the circuit. If a subsystem lies on the critical path, low VTH transistors Implementing the sub-system design while High VTH transistors based sub-systems are used on non-critical paths. Where,μ0 is the zero bias mobility, oxide capacitance is represents as Cox, and (W/L) represents the width to the length ratio of the leaking MOS device. The subthreshold current flows due to three main reasons: Drain Induced Barrier Lowering (DIBL)effect, weak inversion effect and the direct punch-through of the electrons between drain and source. The DIBL effect occurs at higher drain voltages where threshold voltage of transistor reduces. Depletion region of the p-n junction between the drain and body increases with the increase in drain voltages which increases more under the gate voltage. Responsibility to balance the electron charges in depletion region is more on drain voltage rather than gate voltage. For this kind of arrangement they would not affect the circuit timing and hence performance as well as leakage optimization can be achieved. Two kinds of algorithm are used such as exact or Heuristics.

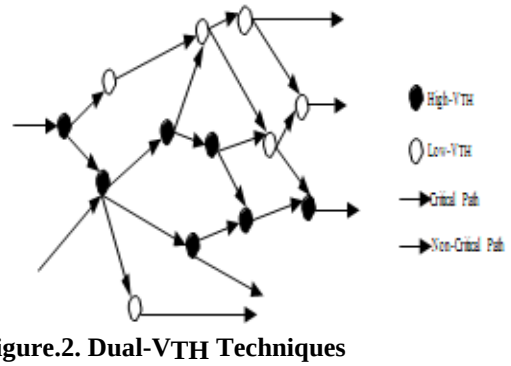

Figure.2. Dual-VTH Techniques

2.2 Transistor Stacking Technique

Transistor stacking is a run time leakage reduction technique In which, a single transistor divide into two half size transistor. The purpose of this kind of arrangement is to increase the number of off transistor in stack. If two transistors are off instead of single off transistor highly reduces the leakage. ISUB is exponentially depends on the potential at each terminal every in CMOS.Fig.3.depicts the effect of self-reverse bias when gate terminal potential is at ground, and variation of drain current is occur [9].

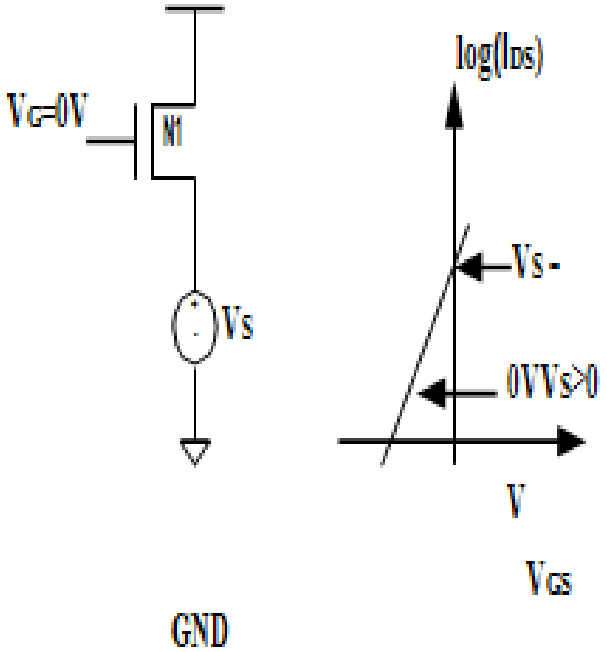

Figure.3.Self-Reverse biasing effects on ISUB

2.3. Power Gating Technique

Power gating technique cut-off the logic circuit from Vdd to GND for reduction in subthreshold leakage current, which flows from the power supply towards ground due to non-ideal characteristics (finite resistance) of CMOS transistor. This technique uses the power supply voltage as the primary source for minimizing leakage current. It inserts an extra MOS switch as a sleep transistor to cut off, or gate, a circuit from the power rails (VDD and/or GND) during standby mode. The additional sleep switch is connected typically as header between the circuit and the VDD or as footer between the circuit and the GND [10].

2.4. Body Bias Technique

It is a run time leakage reduction technique which utilizes the body(substrate) terminal of the MOS transistor to dynamically modify the VTH of a transistor during circuit operation. Depending upon the polarity of the voltage difference between the source and body terminals (VSB),the VTH can be either increased. The VTH is increased when the source-to-substrate p–n junction of a MOSFET is reversing biased called Reverse Body Biasing (RBB)[11-12]. The VTH of a MOSFET can be reduced by forward biasing the source-to-substrate p–n junction called Forward Body Biasing (FBB). RBB for CMOS; 45nm PTM[11] file issued here. For leakage reduction RBB is preferred because it increases the VTH which results leakage reduction of the logic circuit.

- Reduced complexity of logic and hence, lower Capacitance, and faster speed.
- The power consumption is usually higher than conventional CMOS design, because static current always flows through logic gate whenever the pull- down network is on.

Better suited for large fan-in gates because each input connects to a single transistor, presenting a smaller load to the preceding gate.\ When a source terminal is biased of an NMOS transistor, it reduces ISUB exponentially due to the following facts:Fig.4 stacking of two NMOS transistor. Here width of these NMOS are W/2, W is the width of original NMOS transistor.

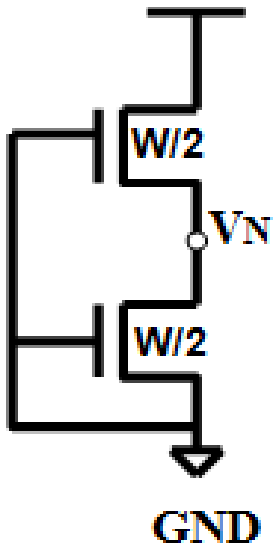

Figure.4.Two NMOS Transistor Stack OFF condition

3.PROPOSED WORK

In this proposed work, operation and structure of low leakage power design stack with pass transistor logic. This proposed circuit design is compared with well-known previous approaches, i.e., Conventional Gates. In the proposed circuit, we have introduced fundamental techniques stack approach with pass transistor approach to reduce the leakage power consumption in the circuit. Here we use combination of two NMOS pass transistor is place below pull up network and PMOS transistor place parallel to the NMOS transistor in between pull up network and pull down network.

The Pull up transistor Turn ON NMOS pass transistor and Pull down transistor turns ON PMOS pass transistor during active mode of the circuit, during sleep both the pass transistor returns of and rail the network from the supply voltage which help in reduction of the leakage power. Similar action also repeats in pull down network the while interchanging the pass transistor NMOS transistor provide the stacking effect (Fig.5.).

To maintain the value “0” in sleep mode operation and PMOS pass transistor connect parallel with NMOS transistor. To maintain an output value to “0” PMOS transistor connected to GND in sleep mode.

To achieve proper Logic at the output NMOS transistor is connect to Vdd and PMOS transistor is connect to GND. The stacking of the transistor reduces the leakage power in proposed approach. To maintain the proper high logic insert NMOS transistor parallel to PMOS stacked transistor in pull up network, to connect sleep transistor to Vdd to the pull up network. In sleep mode, this NMOS Transistor connects Vdd to the pull up network when sleep transistor cutoff.

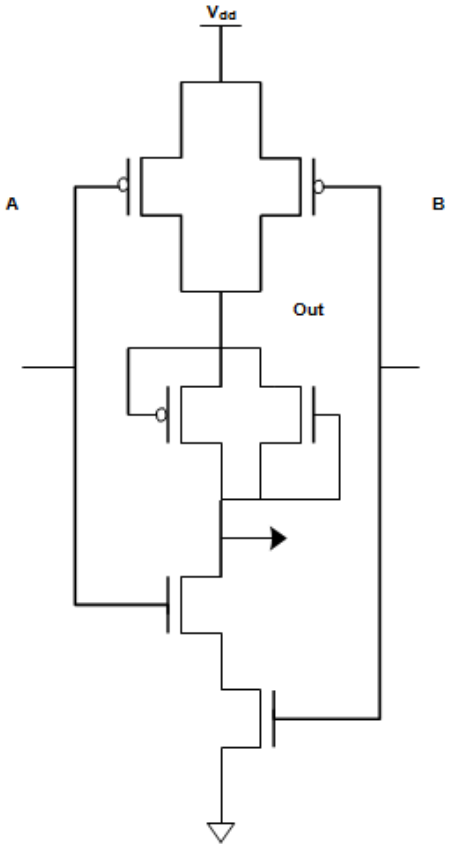

Figure.5.Proposed Circuit

4. TABLES AND DISCUSSION

Leakage current for Proposed circuit is to be calculated by using Berkley Predictive Technology Module (BPTM) in HSPICE simulator using 45nm and 32nm process technology with supply voltage of 0.9v and 0.8V at 10MHz frequency and CL=1pf. Leakage power of conventional gate is given with all input vector combination at 250C and 1000C temperature respectively. Transient analysis of proposed technique will be done with NAND gate.

Table I. Dynamic Power at 45nm 25^0C

Gates	Average Power(μW)	Delay(pS)			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.2057	4.847	5.181	5.014	1.031
AND	0.4163	10.96	5.424	8.192	3.410
NAND	0.2627	8.455	3.352	5.903	1.550
NOR	0.2336	9.279	3.094	6.186	1.445
EXOR	0.3595	6.247	6.572	6.409	2.304

Table II. Dynamic Power at 45nm 100^0C

Gates	Average Power	Delay			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.3048	4.671	5.418	5.044	1.537
AND	0.6534	11.21	5.318	8.264	5.399
NAND	0.3901	8.374	2.779	5.576	2.175
NOR	0.3205	9.810	3.173	6.491	2.080
EXOR	0.4065	6.046	6.874	6.362	2.586

Table III. Dynamic Power at 32nm 25^0C

Gates	Average Power	Delay			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.1440	5.382	5.612	5.497	0.791
AND	0.2708	11.19	5.658	8.424	2.281
NAND	0.1862	9.422	2.694	6.058	1.127
NOR	0.1661	10.73	3.571	7.150	1.187
EXOR	0.1875	11.96	12.83	12.39	2.323

Table IV. Dynamic Power at 32nm 100^0C

Gates	Average Power	Delay			PDP
		T_R	T_F	$T_R+T_F=T_{Total}$	
NOT	0.2210	5.117	5.810	5.463	1.207
AND	0.4534	11.15	5.940	8.545	3.874
NAND	0.2860	9.604	3.053	6.328	1.809
NOR	0.2328	11.06	3.235	7.148	1.664
EXOR	0.2865	10.93	11.58	11.25	3.223

Table V. Leakage Power Consumption at 45nm at 25^0C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	21.83	75.23		
AND	60.45	109.1	76.07	172.8
NAND	31.46	149.8	103.6	150.4
NOR	43.63	83.11	72.86	111.8
EXOR	155.9	108.4	108.4	155.9

Table VI. Leakage Power Consumption at 45nm at 100^0C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	52.00	83.32		
AND	119.3	188.6	152.2	218.9
NAND	39.88	260.2	154.34	166.5
NOR	103.8	95.12	80.98	114.8
EXOR	176.0	166.5	166.5	176.0

Table VII. Leakage Power Consumption at 32nm at 25^0C

Gates	Leakage Power Consumption at 32nm			
	00	01	10	11
NOT	10.14	24.88		
AND	21.34	48.66	30.00	59.92
NAND	3.921	31.21	12.57	49.73
NOR	20.26	24.97	24.33	42.90
EXOR	49.28	43.70	43.70	49.28

5. CONCLUSION

CMOS nanotechnology in meter scale, sub threshold leakage power is compatible to dynamic power consumption, which results as a challenge in handling leakage power. In this paper, we try to present a new approach named "stacking sleepy Approach" to minimize the leakage problem. This proposes a technique in order to reduce the leakage current during idle mode of circuit. The proposed technique can be applied on low power, high performance application, where leakage is the point of major concern such as memory units, microprocessor and other different portable devices. In future, new approach of leakage reduction technique at gate level and block level are to be exploited to give better power saving than the current approaches used in CMOS circuit level design.

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