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Design & Implementation of Improved SRAM Cell

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Abstract:
Static Random Access Memory (SRAM) has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power memory design during recent years due to increase demand for notebooks, laptops, IC memory cards and hand held communication devices. SRAMs are widely used for mobile applications as both on chip and off-chip memories, because of their ease of use and low power consumption. In the performance of memory cell, delay and power consumption plays a major role. The main objective of this project is to design low power consumption SRAM cell and SRAM array for embedded applications.

Keywords: Static Random Access Memory (SRAM), Power Consumption, Delay

I. INTRODUCTION

Static random-access memory is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered. The primary obstacles to the scaling of bulk CMOS to 32nmgatelengths include short channel effects, Sub-threshold leakage, gate-dielectric leakage and device to device variations. Due to sudden increase in threshold voltage i.e. Vt oscillation produced by overall and general process variations occur in ultra-short channel devices, 6T SRAM cell and their modifications cannot be operated at advance scaling of supply voltages without functional and parametric failure causes yield loss. The design of standard 6T SRAM cell undergoes a lot of problem on write delay. The design of Low power 6T SRAM cell could decrease the write power and access delay but could not improve their stability. The main objective of this work is to design a modified SRAM cell with low power consumption.

II. SRAM CELLS AND ITS OPERATION

1. 6T SRAM CELL

The memory cell is the basic building block of any static memory system. Figure 1 shows a conventional 6- transistor static memory cell in CMOS technology. The circuit is a flip-flop comprising two cross-coupled inverters and two access transistors, M5 and M6.

A. STANDBY MODE:

In standby mode word line is not asserted (word line=0), so pass transistors M5 and M6 which connect 6t cell from bit lines are turned off. It means that cell cannot be accessed. The two cross coupled inverters formed by N1-N2 will continue to feedback each other as long as they are connected to the supply, and data will hold in the latch.

B. READ MODE:

The wordline (WL) and bitlines (BL) are held at VDD during read operation. First, the feedback from the cross coupled inverters is broken. Next, the voltage of the inverter formed by half of the SRAM cell is found by sweeping Q (the inverter's input) from 0 to VDD and measuring QB (the inverter's output).

C. WRITE MODE:

During a write operation, VDD is applied to the word line and the value to be written into the memory cell is driven onto the bitlines.Thus, Figure 1 illustrates how to extract the write static noise margin (SNM). Again, feedback from the cross-coupled inverters is broken and the voltage of the inverter is measured. Note however that in this case, the voltages of the two halves of the SRAM are no longer the same (since one the bitlines is driven to 0V, and the other to VDD).

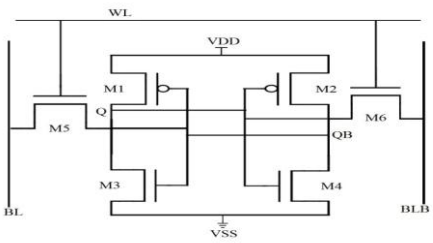

Figure.1. 6T SRAM CELL

2. 7T SRAM CELL

The circuit of 7T SRAM cell is made of two CMOS inverters that are connected cross coupled to each other with additional NMOS Transistor which is connected to read line and has two pass NMOS transistors connected to bit lines and bit line bar respectively.

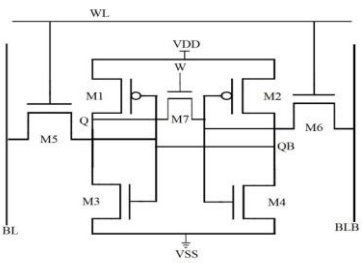

Figure.2. 7T SRAM CELL

Figure 2 shows circuit of 7T SRAM Cell, where the access transistors M5 is connected to the word-line (WL) to perform the access write and M6 is connected to the Read-line (R) to perform the read operations thought the column bit-lines (BL_1 and BL_2). The bit-lines act as I/O nodes carrying the data from SRAM cells to a sense amplifier during read operation or from write in the memory cells during write operations.

3. 8T SRAM CELL

The architecture of 8T SRAM cell is similar to that of conventional 6T SRAM cell. But the pass transistors in 6T SRAM cell are replaced by Transmission Gates. Therefore, two extra transistors M7 and M8 are added to the circuit. The working of TG8T SRAM cell consist of two operation i.e. write and read operation.

A. READ MODE:

When we performing a write operation ,both the bit lines are at opposite voltages which represent if bit line BL is at high then BLB is at low and vice versa (BL=1 and BLB =0 or BL =0 and BLB =1). When WL becomes high and also WLB =0 which enables NMOS and PMOS transistors M5 and M6 then data writes on the output nodes Q and QB of back to back connected inverter.

B. WRITE MODE:

When we perform the read operation which is just opposite to the write operation, both the bit lines are at high voltages also behave as an output and WL is raised to high and WLB at 0. Since one of the output nodes (Q and QB) is at low then one of pre-charged bit lines start discharging and at that instant data is going to be read.

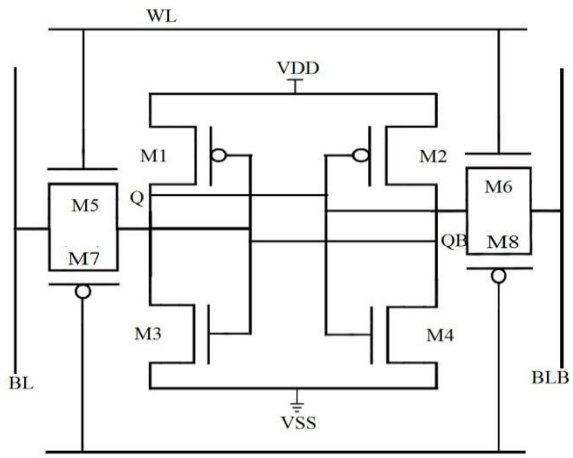

Figure.3. 8T SRAM CELL

4. 9T SRAM CELL:

The cell consists of a 6T SRAM part (the write-access transistors with a cross-coupled latch) and a dedicated read port. The read port comprises three NMOS transistors (M7, M8, and M9) for realizing equalized bitline leakage and improving bitline sensing margin in a single-ended read bitline (RBL).

A. READ MODE:

A read operation starts by enabling a read word line (RWL) and is followed by conditional RBL discharging. If Q holds logic 0, M7 is turned on and discharges RBL to GND. If, on the contrary, Q stores logic 1, M8 is activated and provides pull-up current from RWL ((=V)) to RBL, slowing down the discharging speed of RBL.

B. WRITE MODE:

A write operation is enabled by activating a write word line (WWL) and completed when the data loaded at WBL and WBLB is written into Q and QB.

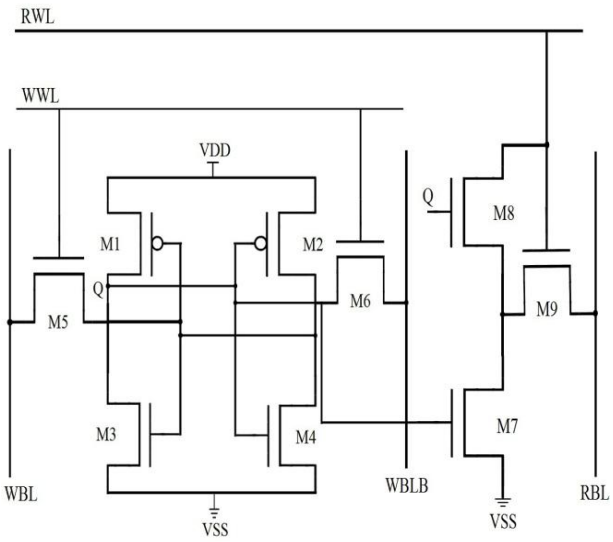

Figure.4. 9T SRAM CELL

III. 4X4 SRAMCELL ARRAY DESIGN

This section describes the designing of 4x4 SRAM cell arrays of 4 rows and 4 columns. Each block of the array is of SRAM cell. There are 4 rows and 4 columns arranged to form a 4x4 SRAM cell array. To address these rows of cells the decoder is used prior to the array arrangement. The AND based 2:4 decoder is used to generate the address lines, the number of transistors used for the decoder circuit is 28 (each AND gate uses 6 transistor and NOT gate made up of 2 transistors).

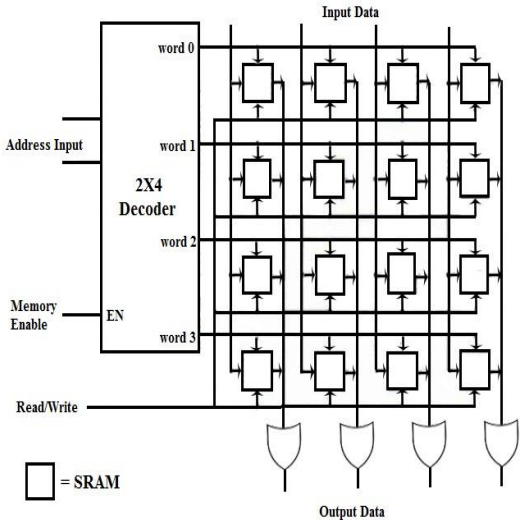

Figure.5. 4X4 SRAM CELL ARRAY

These address lines which form the outputs of decoder are connected to each row of the array. The input and output data control consists of write and ready circuitry. From the decoder the address is selected in the array and 4 bits of data is written or read in parallel from D0 to D3. The SRAM block in the above figure is replaced with 6T SRAM and 7T, 8T and 9T SRAM cells to form array of SRAM cells with respective cells. When the SRAM is replace with 6T SRAM cell, the power consumption and delay are measured. The same is done

with 7T, 8T and 9T SRAM cells as the block component. After the implementation of SRAM array with 6T, 7T, 8T and 9T SRAM cells, the power consumption and delay are compared.

IV. RESULTS

The power consumption and delay of single 6T, 7T, 8T and 9T SRAM cells are compared at different technologies such as 180nm, 65nm and 45nm technologies. Also the power consumption and delay of array of SRAM cells are compared at 180nm, 65nm and 45nm technologies.

Table.1. Comparison of power consumption of single sram cells

	180nm	**65nm**	**45nm**
6 Transistor cell	1.243E-10 Watts	***7.5374E-12 Watts***	3.6746E-09Watts
7 Transistor cell	*1.6267E-10Watts*	5.5713E-11Watts	**3.0864E-12Watts**
8 Transistor cell	8.9148E-11Watts	*4.0717E-10Watts*	**5.0939E-17Watts**
9 Transistor cell	**1.1343E-06Watts**	*3.5644E-06Watts*	3.5644E-06Watts

Table .2. Comparison of delay of single sram cells

	180nm	**65nm**	**45nm**
6Transistorcell	**8.2602fsec**	10nsec	9.9997nsec
7Transistorcell	**268.77fsec**	9.999nsec	1.075psec
8Transistorcell	10nsec	10nsec	**2.0744fsec**
9Transistorcell	**136.26fsec**	5.0003nsec	5.003nsec

Table. 3. Comparison of power consumption of array of sram cells

	180nm	**65nm**	**45nm**
6 Transistor Array	4.9441E-10Watts	5.3700E-10Watts	**2.2273E-10Watts**
7 Transistor Array	2.2711E-08Watts	1.3918E-08Watts	**2.0458E-09Watts**
8 Transistor Array	2.7622E-08Watts	1.4264E-10Watts	**10.253E-12Watts**
9 Transistor Array	8.7091E-04Watts	**3.2137E-07Watts**	**3.2137E-07Watts**

Table .4. Comparison of delay of array of sram cells

	180nm	**65nm**	**45nm**
6 Transistor Array	**70nsec**	**70nsec**	**70nsec**
7 Transistor Array	**69.99nsec**	70nsec	70nsec
8 Transistor Array	70nsec	70nsec	**69.99nsec**
9 Transistor Array	33.235psec	70nsec	**7.3448fsec**

Simulated Waveforms for Single SRAM cell:

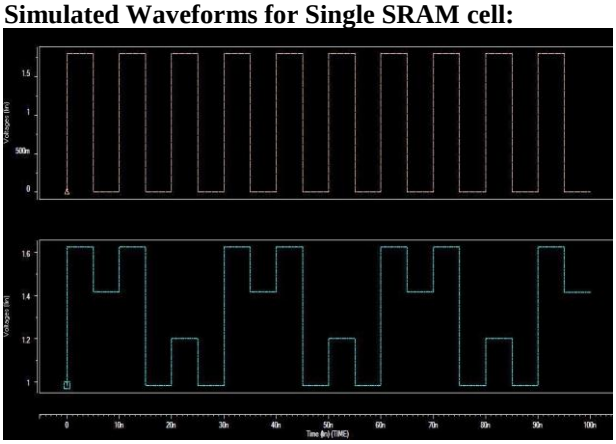

Figure.6. 8t Single Sram Cell Waveform (180nm Technology)

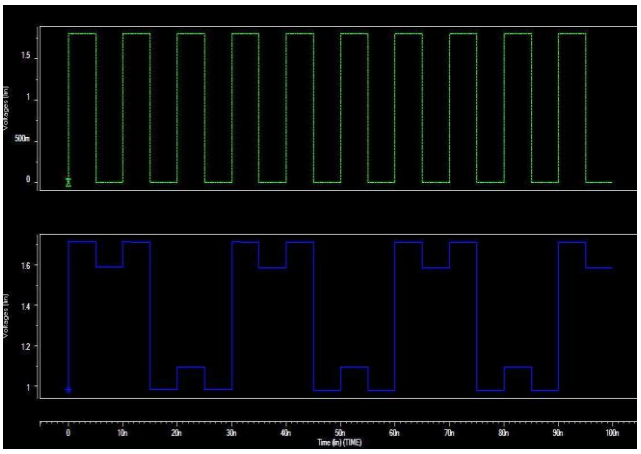

Figure.7. 8T Single Sram Cell Waveform (65nm Technology)

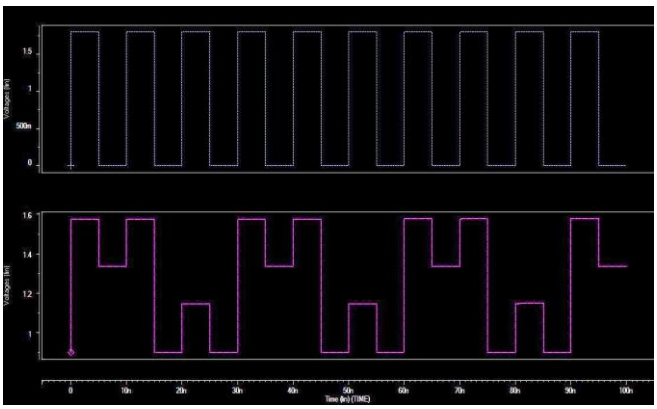

Figure.8. 8t single sram cell waveform (45nm technology)

Simulated Waveforms for Array of SRAM cells:
8 Transistor array:

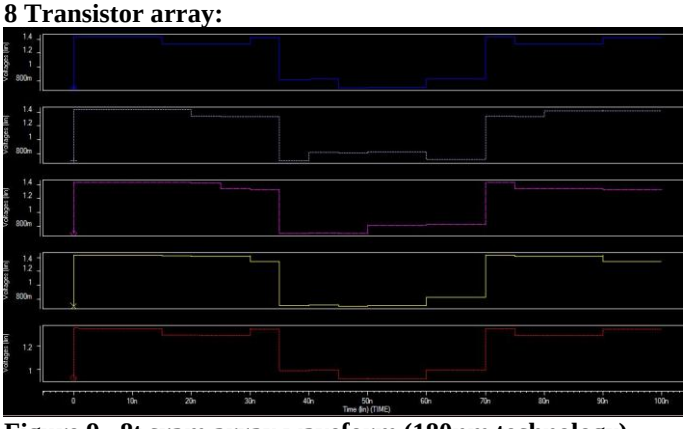

Figure.9. 8t sram array waveform (180nm technology)

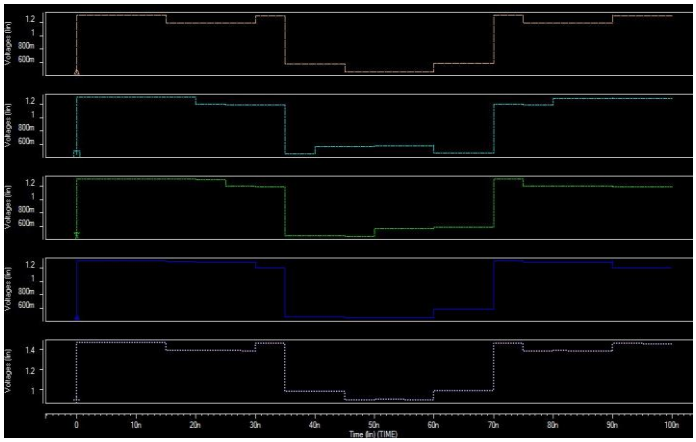

Figure. 10. 8T SRAM array waveform (65nm technology)

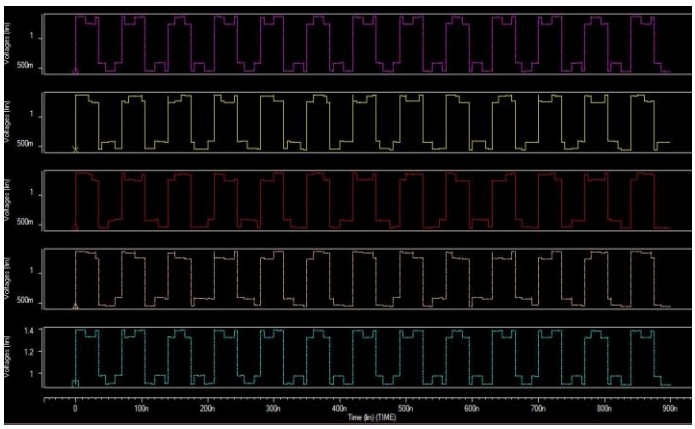

Figure.11. 8T SRAM Array Waveform (45nm Technology)

V. CONCLUSION

The conventional 6T SRAM cell is implemented in 180, 65 and 45nm technologies and compared with 7T, 8T and 9T SRAM cells in terms of power. By the comparison of conventional 6T SRAM Cell and 4X4 array with 7T, 8T and 9T SRAM cells with the help of HSpice tool, the 8T SRAM single cell and 4X4 array with transmission gate consumes low power.

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