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A Comparison of Seven-Level Inverter Topologies with Minimum Number of Switches for Induction Motor Drive

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Abstract:
Multilevel inverter is used in applications that need high voltage and high current. However the main drawback of MLI is their increased number of power devices, passive components, complex pulse width modulation control and balancing of capacitor voltages. In this paper two popular topologies such as Reversing Voltage Multi-Level Inverter and Cascaded Multi-Level Inverter based on Developed H-Bridge inverter are discussed. When compared with existing inverters, fewer components (particularly in higher levels) are sufficient and require fewer carrier signals and gate drives. The operating principle of each topology and the analysis of the two MLI are included. Simulation study of these topologies considered is carried out on MATLAB/SIMULINK platform for Induction Motor drive.

Keywords: Multi Level Inverters, Cascaded multilevel inverter, developed H-bridge, RVMLI, THD, IPD PWM.

I. INTRODUCTION

A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy. In recent years, there has been a substantial increase in interest to multilevel power conversion. The term multilevel began with the three-level converter. The advantages of three-level Inverter topology over conventional two-level topology are:

1. The voltage across the switches is only one half of the DC source voltage;

2. The switching frequency can be reduced for the same switching losses;

3. The higher output current harmonics are reduced by the same switching frequency.

Recent research has involved the introduction of novel converter topologies and unique modulation strategies. However, the most recently used inverter topologies, which are mainly addressed as applicable multilevel inverters, are cascade converter, neutral-point clamped(NPC) inverter, and flying capacitor inverter. There are also some combinations of the mentioned topologies as series combination of a two-level converter with a three-level NPC converter which is named cascade 3/2 multilevel inverter[3]. There is also a series combination of a three-level cascade converter with a five-level NPC converter which is named cascade 5/3 multilevel inverter [4]. The proposed topology is a symmetrical topology since all the values of all voltage sources are equal. However, there area symmetrical topologies [5] which require different voltage sources. This criterion needs to arrange dc power supplies according to a specific relation between the supplies. Difference in ratings of the switches in the topology is also a major drawback of the topology. This problem also happens in similar topologies [6]–[8], while some of the high-frequency switches should approximately withstand the maximum overall voltage which makes its application limited for high-voltage products. In practical implementation, reducing the number of switches and gate driver circuits is very important. Reversing Voltage Multi-Level Inverter (RVMLI) and Cascaded Multi-Level Inverter based on Developed H-Bridge (CMLIDHB) inverter will obtain a nearly sinusoidal voltage with a lower switch count [1][14]. Single phase AC supply obtained from this topology is given to single phase Induction Motor and are the most common domestic appliance due to their rugged construction and lower cost. Also this topology can be easily implemented for three phase system due to less number of switches and hence less complexity of controlling them.

II. CIRCUIT TOPOLOGY

a) Reversing Voltage Multi-Level Inverter

The power circuit of the inverter consists of the power semiconductors witches which are combined to produce a high-frequency wave form in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology[1].This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named *level generation* part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability. The other part is called *polarity generation* part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency. The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output. In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities. The RV topology in seven levels is shown in Fig. 1. As can be seen, it requires ten switches and three isolated sources. The principal idea of this topology as a multilevel inverter is that the left stage in Fig. 1 generates the required output levels (without polarity) and the

right circuit (full-bridge converter) decides about the polarity of the output voltage. This part, which is named polarity generation, transfers the required output level to the output with the same direction or opposite direction according to the required output polarity. It reverses the voltage direction when the voltage polarity requires to be changed for negative polarity.

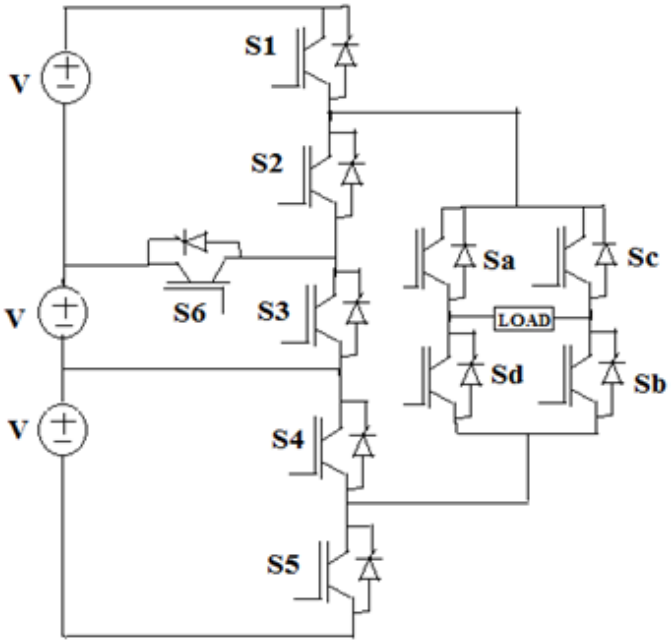

Figure.1.Seven level structure of RVMLI.

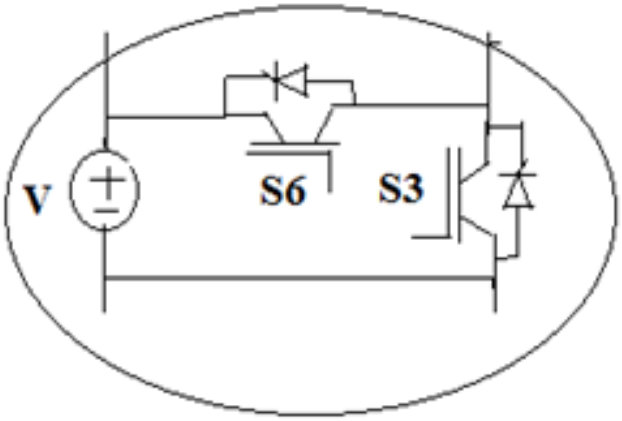

Figure.2. RVMLI duplicate stage for higher levels.

This topology easily extends to higher voltage levels by duplicating the middle stage as shown in Fig. 1. Therefore, this topology is modular and can be easily increased to higher voltage levels by adding the middle stage in Fig. 2. Hence the higher levels are obtained easily and with fewer components. Switching sequences in this converter are easier than its counter parts. According to its inherent advantages, it does not need to generate negative pulses for negative cycle control. Thus, there is no need for extra conditions for controlling the negative voltage. Instead, the reversing full-bridge converter performs this task, and the required level is produced by the high-switching-frequency component of the inverter. Then, this level is translated to negative or positive according to output voltage requirements. This topology is redundant and flexible in the switching sequence. In this paper, IPD SPWM is adopted for its simplicity. Carriers in this method do not have any coincidence, and they have definite offset from each other. They are also in phase with each other. The modulator and three carriers for SPWM are shown in below Fig.

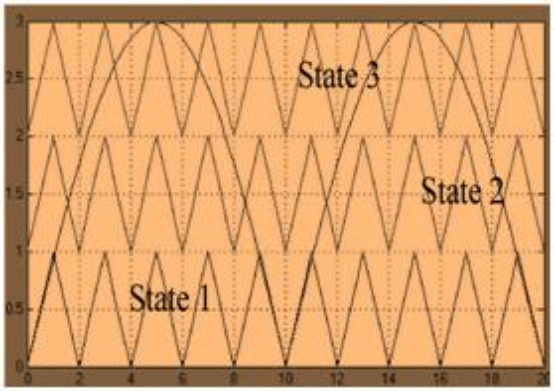

Figure.3. IPD PWM structure of RVMLI

b) Cascaded Multi-Level Inverter based on Developed H-Bridge

As shown in Fig. 4, the CMLIDHB topology [14] is obtained by adding two unidirectional power switches and one dc voltage source to the H-bridge inverter structure. In other words, the proposed inverters are comprised of six unidirectional power switches (*Sa*, *Sb*, *SL*,1, *SL*,2, *SR*,1, and *SR*,2) and two dc voltage sources (*VL*,1 and *VR*,1). As shown in Fig. 4, the simultaneous turn-on of *SL*,1 and *SL*,2 (or *SR*,1 and *SR*,2) causes the voltage sources to short-circuit. Therefore, the simultaneous turn-on of the mentioned switches must be avoided. In addition, *Sa*and *Sb*should not turn on, simultaneously. Therefore, the values of dc voltage sources should be different to generate more voltage levels without increasing the number of switches and dc voltage sources.

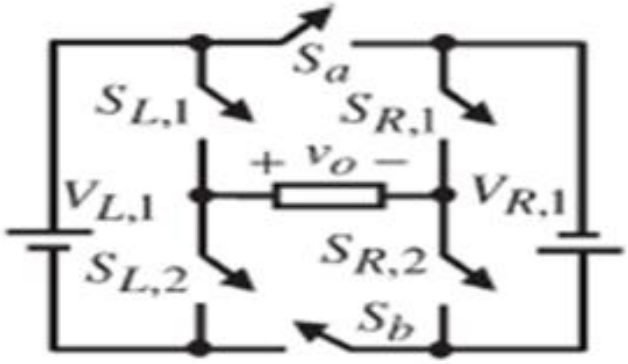

Figure.4. Seven level structure of CMLIDHB.

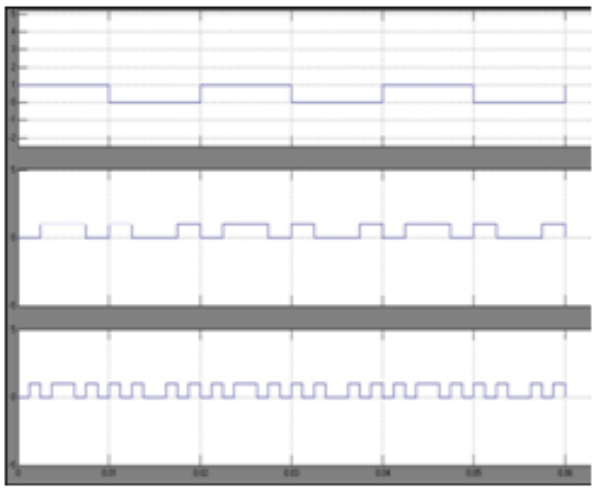

Figure.5. Triggering pulses for switches Sb, Sl2, Sr2.

Fig. 5 shows Triggering pulses for switches Sb, Sl2, Sr2.The pulses for the Sa, Sr1 and Sl1 are invert pulses of Sb,Sr2 and Sl2 respectively. The number of output voltage levels (*N*step), number of switches (*N*switch), number of dc voltage sources

(*N*source), and the maximum magnitude of the generated voltage (*Vo*,max) are calculated as follows, respectively:

$N_{step} = 2^{2n+1} - 1$

$N_{switch} = 4n + 2$

$N_{source} = 2n$

$V_{o,max} = V_{L,n} + V_{R,n}$.

The other important parameters of the total cost of a multilevel inverter for evaluation are the variety of the values ofdc voltage sources and the value of the blocking voltage of the switches. As the variety of dc voltage sources and the value of the blocking voltage of the switches are low, the inverter's total cost decreases [20]. The number of variety of the values of dcvoltage sources (Nvariety) is given by

$N_{variety} = 2n$.

The following pattern is utilized to calculate the maximum magnitude of the blocking voltage of the power switches. As shown in Fig. 1 the blocking voltage of *SR*,1and *SR*,2 are calculated as follows:

*V*SR,1= *V*SR,2 = *VR*,1

where*V*SR,1 and *V*SR,2 indicate the maximum blocking voltages of *SR*,1 and *SR*,2, respectively.

The blocking voltage of *SL*,1and *SL*,2 are as follows:

*V*SL,1= *V*SL,2 = *VL*,1

where*V*SL,1 and *V*SL,2 indicate the maximum blocking voltages of *SL*,1 and *SL*,2, respectively.

Therefore, the maximum blocking voltage of all switches in the proposed seven-level inverter (*V*block,1) is calculated as follows:

*V*block,1=*V*SR,1 + *V*SR,2 + *V*SL,1 + *V*SL,2 + *V*Sa+ *V*Sa

=4(*VR*,1+ *VL*,1).

The magnitudes of the dc voltage sources of the seven-level inverter shown in Fig. 1(b) are determined as follows:

VL,1=*V*dc

VR,1=2*V*dc.

the seven-level CMLIDHB can generate 0, ±Vdc, ±2Vdc, and ±3Vdc at output.

Table .1.Comparison of different types of MLI for 7-level output voltage.

S. NO	Type of equipmen trequired	DC MI	FC MI	Casc aded H bridg e	RVM LI	CMLID HB
1	Sources	1	1	1	3	2
2	Switches	12	12	12	10	6
3	Diodes	30	0	0	0	0
4	DC capacitors	6	6	0	0	0

The total components required for seven level output voltage of different multi-level inverter topologies are tabulated in table 1. Therefore the Reversing Voltage Multi-Level Inverter and Cascaded Multi-Level Inverter based on Developed H-Bridge requires very less device count compared with conventional multi-level inverters.

III. SIMULATION RESULTS

The RVMLI, CMLIDHB have been implemented and simulated using MATLAB for Resistance& Induction motors as loads. The THD of 3.55% for seven level topology with filter has been obtained and shown in fig.10 and the results with Induction Motor load are shown in figures (9,11,12, 13, 15 & 16).

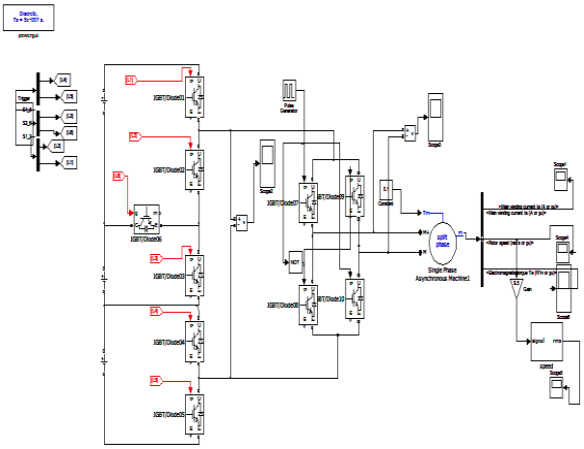

Figure.6. Simulation Circuit for RVMLI fed single-phase Induction Motor.

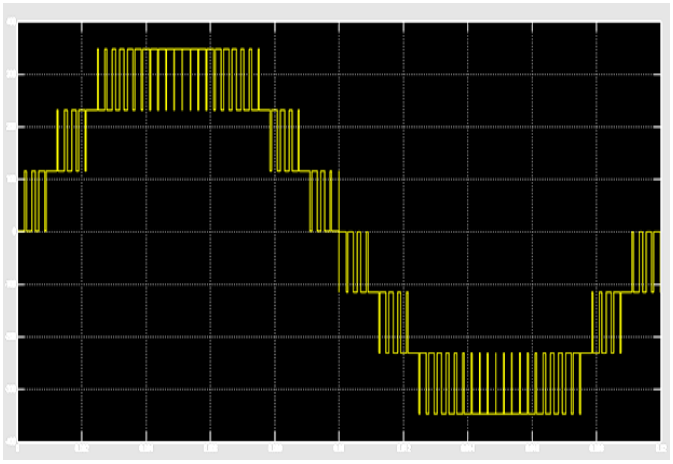

Figure.7.output voltage waveform of RVMLI with R-load without filter

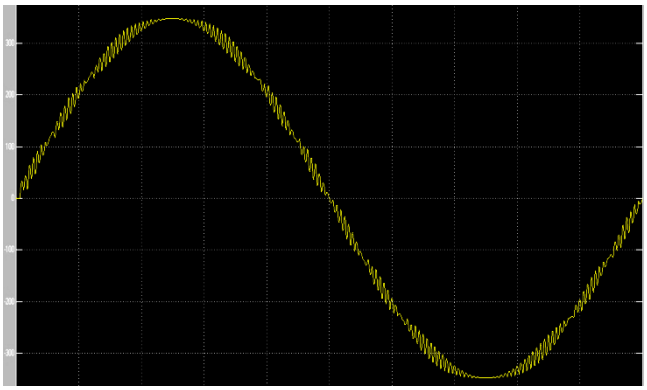

Figure.8. output voltage waveform of RVMLI with R-load with filter

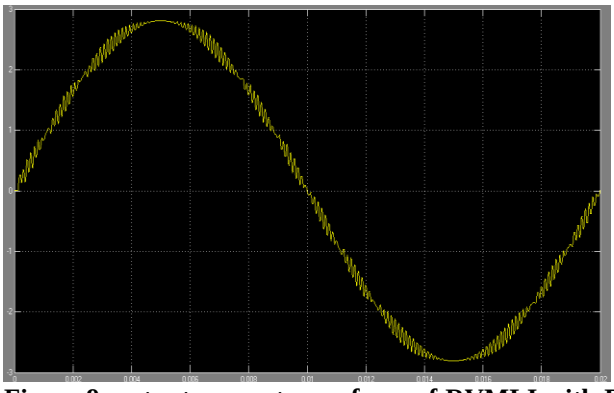

Figure.9. output current waveform of RVMLI with R-load with filter

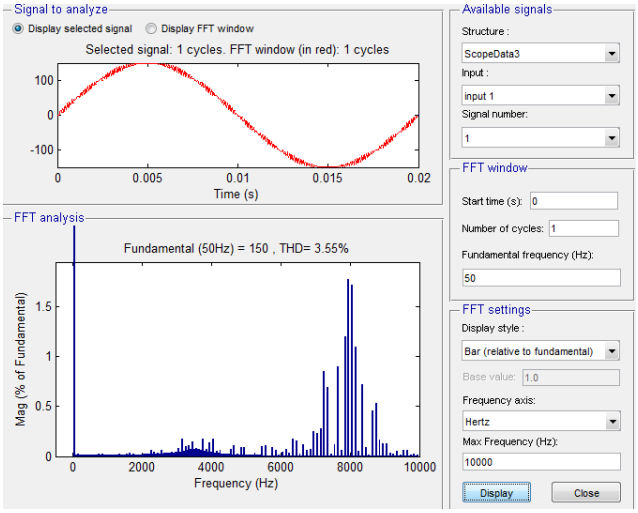

Figure. 10.FFT Analysis

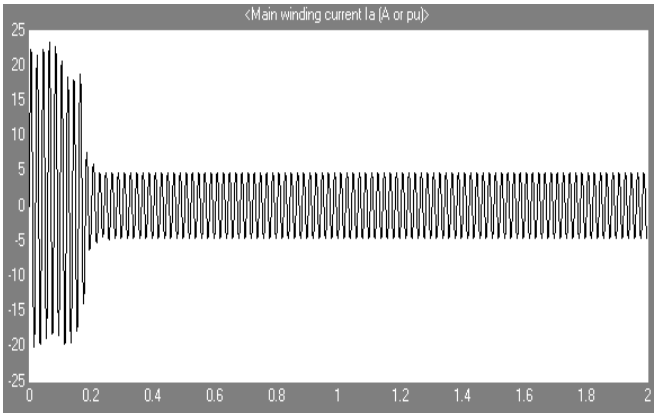

Figure.11.Stator current waveform of RVMLI fed single phase induction motor.

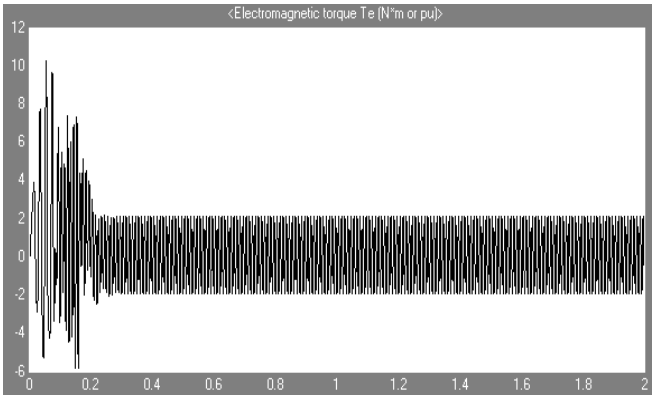

Figure.12.Torque waveform of RVMLI fed single phase induction motor.

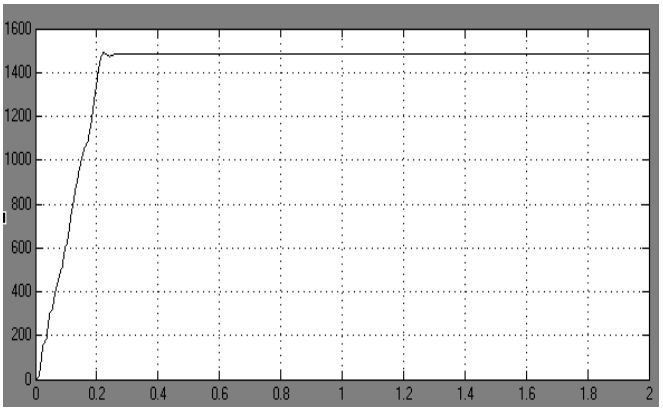

Figure.13 speed waveform of RVMLI fed single phase induction motor.

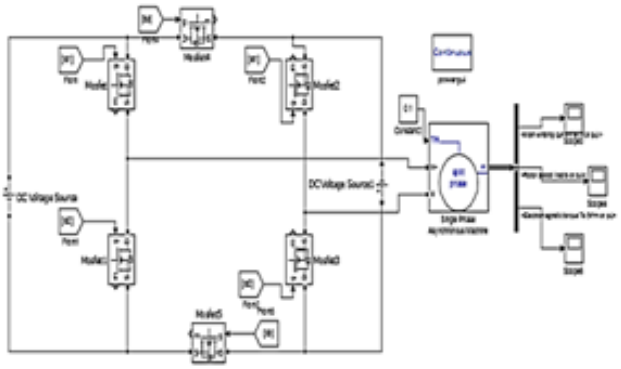

Figure.14 Simulation Circuit for CMLIDHB fed single-phase Induction Motor.

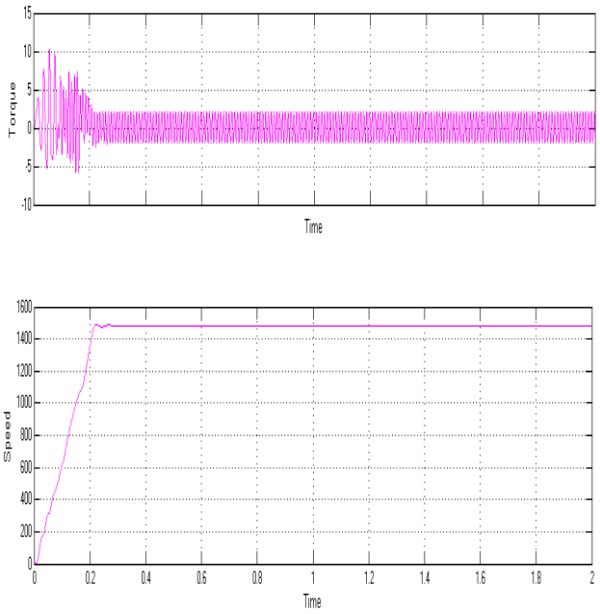

Figure.15.Torque and speed waveform of CMLIDHB fed single phase induction motor.

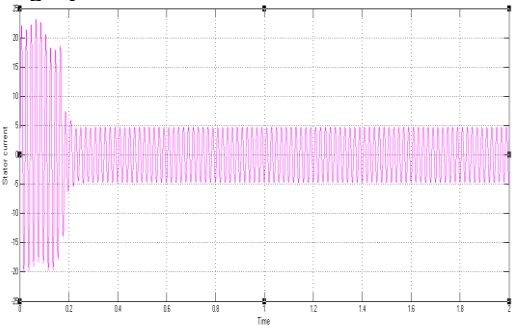

Figure.16.Stator current waveform of CMLIDHB fed single phase induction motor.

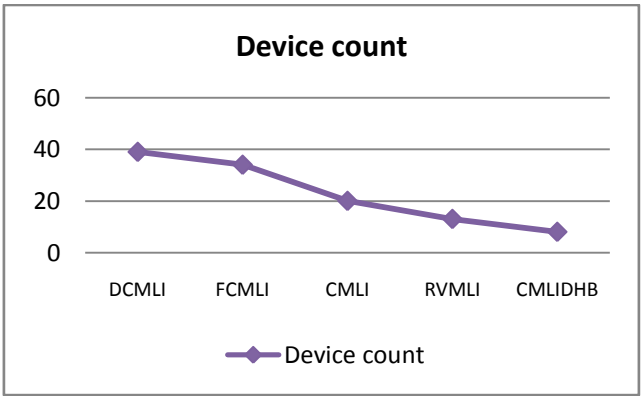

Figure.17. Comparison of device count between different Multi level structures.

IV. CONCLUSION

In RV (Reversing Voltage) multilevel inverter topology, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost. The CMLIDHB with few components will further reduce the complexity and cost. These topologies are very suitable for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc The RVMLI and CMLIDHB topologies provides the better sinusoidal output voltage with low THD and also requirement of gate drivers, protection circuits, installation area and converter cost is reduced compared with existing MLI topologies. In this paper, a single phase Induction Motoris driven for constant torque and simulation results are obtained using the two topologies.

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