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Implementation of Test Pattern Techniques Using BIST Architecture

Allanki Rohith[1], A. Venugopala Rao[2]
M.Tech Student[1], Assistant Professor[2]
Department of Electronics & Communication Engineering
BVC College of Engineering, Rajahmundry, India

Abstract:
BIST is a design-for-testability technique that places the testing functions physically with the circuit under test (CUT). This can perform fault analysis and reduce the power of a circuit during test by generating three intermediate patterns between the random patterns by reducing the hardware utilization. The goal of having LFSR and LP-LFSR patterns is to reduce the transitional activities of Primary Inputs (PI) which eventually reduces the switching activities inside the Circuit under Test (CUT). Here for existing method we will introduce LFSR and for proposed method we will initiate LP-LFSR. Here, the main differentiation will be opt between the existing and proposed methods, the variation for these two methods will be done on power consumption and delay which gives the rate of accuracy. For, this we will use xilinx 14.2 tool and language is Verilog HDL.

Keywords: LFSR, Optimization, Low Power, Test Pattern Generation, BIST

I.INTRODUCTION

The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a response analyzer, and a test controller. The test pattern generator generates the test patterns for the CUT. Examples of pattern generators are a ROM with stored patterns, a counter, and a linear feedback shift register (LFSR). A typical response analyzer is a comparator with stored responses or an LFSR used as a signature analyzer. It compacts and analyzes the test responses to determine correctness of the CUT. A test control block is necessary to activate the test and analyze the responses. However, in general, several test-related functions can be executed through a test controller circuit. During test mode, a test pattern generator circuit applies a sequence of test patterns to the CUT, and the test responses are evaluated by a output response compactor. In the most common type of BIST, test responses are compacted in output response compactor to form (fault) signatures. The response signatures are compared with reference golden signatures generated or stored onchip,and the error signal indicates whether chip is good or faulty. Four primary parameters must be considered in developing a BIST methodology for embedded systems; these correspond with the design parameters for on-line testing techniques discussed in earlier chapter [2].Fault coverage: This is the fraction of faults of interest that can be exposed by the test patterns produced by pattern generator and detected by output response monitor. In presence of input bit stream errors there is a chance that the computed signature matches the golden signature, and the circuit is reported as fault free. This undesirable property is called masking or aliasing. Test set size: This is the number of test patterns produced by the test generator, and is closely linked to fault coverage: generally, large test sets imply high fault coverage. Hardware overhead: The extra hardware required for BIST is considered to be overhead. In most embedded systems, high hardware overhead is not acceptable. Performance overhead: This refers to the impact of BIST hardware on normal circuit performance such as its worst-case (critical) path delays. Overhead of this type is sometimes more important than hardware overhead.

LFSR:
In computing, a linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is exclusive-or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle. Applications of LFSRs include generating pseudo-random numbers, pseudo-noise sequences, fast digital counters, and whitening sequences. Both hardware and software implementations of LFSRs are common. The mathematics of a cyclic redundancy check, used to provide a quick check against transmission errors, are closely related to those of an LFSR.

Applications of LFSR:
- Pattern generator,
- Low power testing,
- Data compression, and
- Pseudo Random Bit Sequences (PRBS).

II.BIST ARCHITECTURE

BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external ATE. Recently, techniques to cope

with the power and energy problems during BIST have appeared. A brief overview of these techniques is given in Section 2. In this paper, we address the low power testing problem in BIST. BIST is well known for its numerous advantages such as improved testability, at-clock-speed test of modules, reduced need for automatic test equipment, and support during system maintenance. Moreover, with the emergence of core-based SOC designs, BIST represents one of the most favorable testing method since it allows to preserve the intellectual property of the design. In most complex SOC designs characterized by very poor controllability and observability, BIST is even probably the only practical solution for efficient testing. The industrial needs initiated academic research. Hence, techniques to cope with the power and energy problems during BIST have appeared recently. These approaches targeting combinational circuits can be classified as follows:

1) Distributed BIST Control Schemes. The goal in these approaches is to determine the BIST blocks of a complex design to be activated in parallel at each stage of the test session in order to reduce the number of concurrently tested modules. The average power is reduced and consequently, the temperature related problems avoided by the increase of the test time duration. On the other hand, the total energy remains constant and the autonomy of the system is not increased.

2) Vector Filtering Architectures as each vector applied to the CUT consumes power but not every vector generated by the pseudo-random TPG contributes to the final fault coverage, the vector filtering architectures consist in preventing application of non-detecting vectors to the CUT. This approach is very effective in reducing power without reducing fault coverage, but does not preserve the CUT from excessive peak power consumption and can lead to high area overhead.

3) Low Power Test Pattern Generators. TPGs based either on LFSRs or Cellular Automata (CA) are carefully designed to reduce the activity at circuit inputs, thus reducing power consumption. These approaches effectively reduce power during test but sometimes at a cost of sub-optimal fault coverage and with no reduction of the peak power consumption.

4) Circuit Partitioning for Low Power BIST [22]. This approach consists in partitioning the original circuit into structural sub-circuits so that each sub-circuit can be successively tested through different BIST sessions. In partitioning the circuit and planning the test session, the average power, the peak power and the energy consumption during BIST are minimized at a low expense in terms of area overhead and with no loss of fault coverage. The only drawback of this approach is that it requires circuit design modification.

The above mentioned approaches can be easily adapted for testing sequential circuits though customized full-scan architectures.

III.IMPLEMENTATION OF BIST

The reduction of the power consumption in a test-per-clock BIST environment is commonly achieved by reducing the switching activity in the CUT. Furthermore, it has been demonstrated in [5] that the switching activity in a time interval (i.e. The average power) dissipated in a CUT during BIST is proportional to the transition density at the circuit inputs. Thereby, several low power test pattern generators have been proposed to reduce the activity at circuit inputs (see above description in part 2.2). Among these techniques, the DS-LFSR proposed in [5] consists in using two LFSRs, a slow LFSR and a normal speed LFSR, as TPG. Inputs driven by the slow LFSR are those which may cause more transitions in the circuit. Although this technique reduces the average power consumption while maintaining a good fault coverage level, the peak power consumption cannot be reduced in practice (a full bit changing may occur at circuit inputs every d clock cycles where d = normal clock speed / slow clock speed). This point represents a severe limitation of the method as the peak power consumption is a critical parameter that determines the electrical limits of the circuit and the packaging requirements. A typical BIST architecture consists of Test Pattern Generator (TPG) usually implemented as a LFSR, Test Response Analyzer (TRA), Multiple Input Signature Register (MISR), CUT and BIST control unit as shown in figure 1.

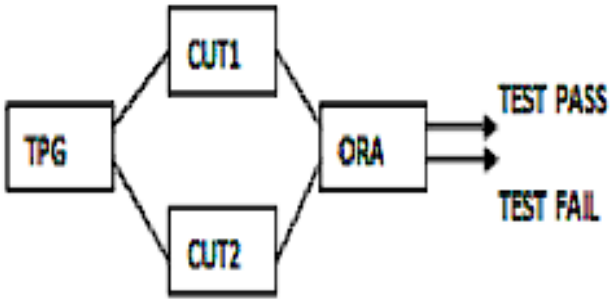

Figure.1. Modified BIST Architecture

CUT: It is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. Their Primary Input (PI) and Primary output (P0) delimit it.TPG: It generates the test patterns for the CUT. It is dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically. MISR: It is designed for signature analysis, which is a technique for data compression. MISR efficiently map different input streams to different signatures with every small probability of alias. TRA: It will check the output of MISR & verify with the input of LFSR & give the result as error or not BIST Control Unit: Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to LFSR, Control MISR & TRA. It will generate interrupt if an error occurs .In BIST, LFSR generates pseudorandom test patterns for primary inputs (PIs) or scan chains input. MISR compacts test responses received from primary output or scan chains output. Test vectors applied to a CUT at nominal operating frequency, often cause more average and/or peak power dissipation than in normal mode. The result in more switching‟s and power dissipation in test mode. As in, the low power/energy BIST technique proposed in this paper is based on a modified clock scheme for the pseudo-random TPG. Basically, a clock whose speed is half of the normal speed is used to activate one half of the D flip-flops in the TPG (i.e. a modified LFSR) during one clock cycle. During the next clock cycle, the second half of the D flip-flops is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with a master clock CLK and have the same but shifted in time period. The clock CLK is the clock of the circuit in the normal mode and has a period equal to T. The basic scheme of the proposed low power test pattern generator with the corresponding

clock waveforms are depicted in Figure 1. As one can observe, a test vector is applied to the CUT at each clock cycle of the test session. However, only one half of the circuit inputs can be activated during this time. Consequently, the switching activity in a time interval (i.e. the average power) as well as the peak power consumed in the CUT are minimized.

The low power TPG:

The idea behind the use of such a low power TPG is to reduce the number of transitions on primary inputs at each clock cycle of the test session, hence reducing the overall switching activity generated in the CUT. Let us consider a CUT with n primary inputs. A n-stage primitive polynomial LFSR with a clock CLK would be used in a conventional pseudorandom BIST scheme. Here, we use a modified LFSR composed of n D-type flip-flops and two clocks CLK/2 and CLK/2_ , and constructed as depicted in Figure 2 (n=6 in the example of Figure 2). As one can observe, this modified LFSR is actually a combination of two n/2-stage primitive polynomial LFSRs, each of them being driven by a single clock CLK/2 or CLK/2_ . The D cells belonging to the first LFSR (referred to as LFSR-1 in the sequel) are interleaved with the cells of the second LFSR (referred to as LFSR-2 in the sequel), thus allowing to better distribute the signal activity at the inputs of the CUT.

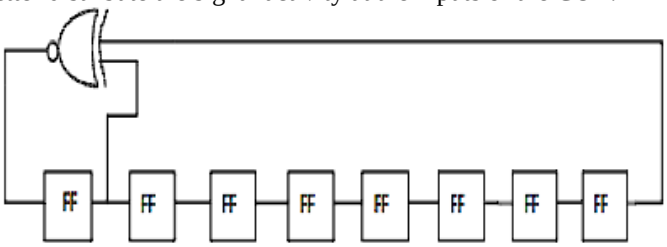

Figure .2. An example of the modified LFSR TPG

In order to better describe the functioning of the low power TPG, the timing diagram of the test sequence generated by the example TPG shown in Figure 2 is reported in Table 1. Assume that the seed <001> has been chosen for both LFSRs, such that the first vector applied to the CUT at time T is <100001>. Only LFSR-1 is active during the first clock cycle (LFSR-2 is in stand-by mode). This is illustrated in the two last columns of Table 1 in which a 8 grey cell represents the active LFSR in the corresponding clock cycle. During the next clock cycle, LFSR-2 is active (LFSR-1 is in stand-by mode) and vector <110000> is applied to the CUT. The advantage of the modified LFSR composed of two interleaved *n/2*-stage LFSRs (over a simpler structure composed of two separated *n/2*-stage LFSRs) is that it allows to better distribute the signal activity at the circuit inputs during the BIST session. This is particularly important for circuits in which the input cones of the primary outputs are highly non -overlapping. In this case, two separated LFSRs would activate only one part of the circuit in a given time interval, instead of the whole circuit with the proposed structure in which two LFSRs are interleaved. Shorter test lengths to reach a target fault coverage can hence be predicted with the proposed interleaved LFSR structure.

Implementing algorithm for LT-LFSR

The proposed approach consists of two half circuits. The algorithm steps says the functions of both half circuits is

Step1: First half is active and second half is idle and gives out is previous; the generating test vector is Ti.

Step2: Both halves are idle First half sent to the output and second half‟s output is sent by the injection circuit, the generating test vector is Ti1.

Step3: Second half is active First half is in idle mode and gives out as previous, the generating test vector is Ti2.

Step4:Both halves are in idle mode, First half is given by injection circuit and Second half is same as previous, the generating test vector is Ti3.

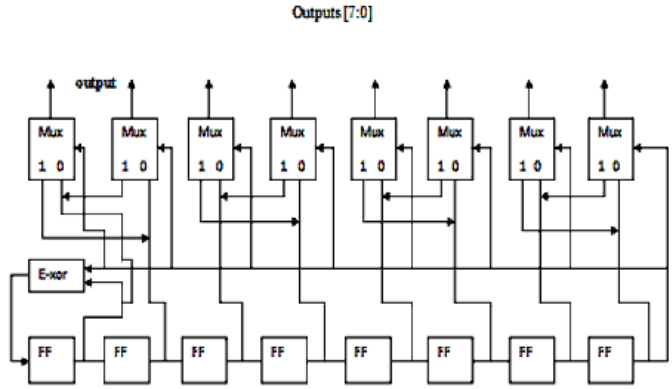

Figure.3. LP-LFSR

After completing step 4 again goes to step1 for generating test vector Ti+1. The first level of hierarchy from top to down includes logic circuit design for propagation either the present or next state of flip- flop to second level of hierarchy. Second level of hierarchy is implementing Multiplexed (MUX) function i.e. selecting two states to propagate to output which provides more power reduction compared to having only one of the R Injection and Bipartite LFSR techniques in a LFSR due to high randomness of the inserted patterns..

IV. IMPLEMENTATION RESULTS

The following figures are the existing and proposed methods waveforms and RTL.

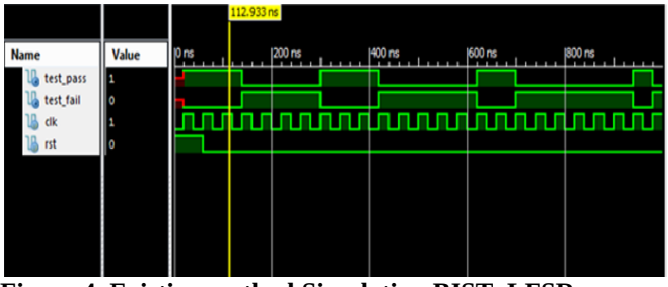

Figure.4. Existing method Simulation BIST_LFSR

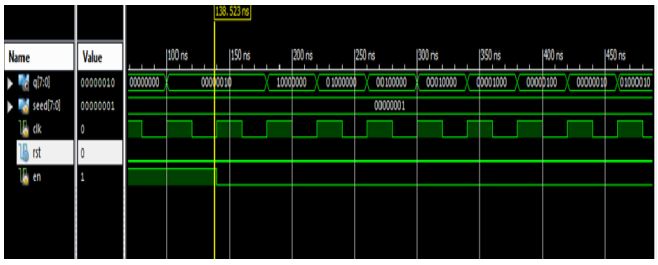

Figure.5. Proposed method Simulation BIST_LP-LFSR

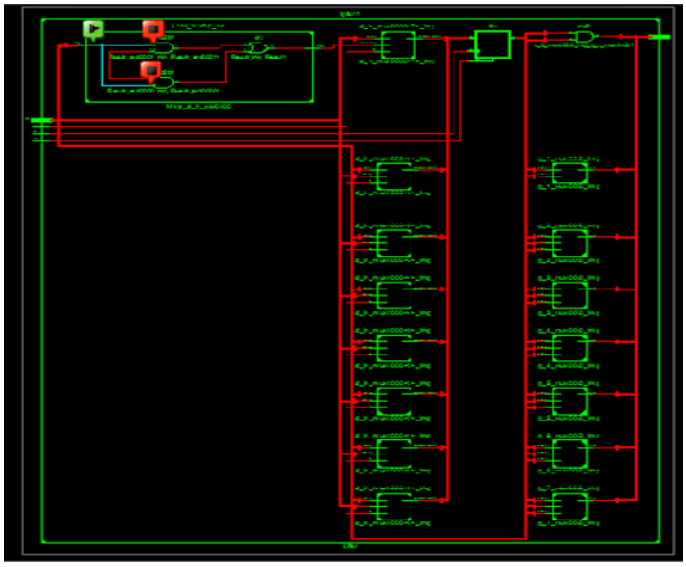

Figure.6. Proposed RTL for BIST_LP-LFSR

AREA:-

The following figures are the existing and proposed synthesis reports as shown below**:-**

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	62	4656	1%
Number of Slice Flip Flops	38	9312	0%
Number of 4 input LUTs	112	9312	1%
Number of bonded IOBs	19	232	8%
Number of MULT18X18SIOs	1	20	5%
Number of GCLKs	1	24	4%

Figure .7. Existing Method Area

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	34	4656	0%
Number of Slice Flip Flops	10	9312	0%
Number of 4 input LUTs	60	9312	0%
Number of bonded IOBs	13	232	5%
Number of GCLKs	1	24	4%

Figure.7. Proposed Method Area

DELAY:-

```
=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 3 / 1
-------------------------------------------------------------------------
Delay:               6.209ns (Levels of Logic = 3)
  Source:            ti (PAD)
  Destination:       tout (PAD)

  Data Path: ti to tout
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.218   0.595  ti_IBUF (ti_IBUF)
     LUT3:I0->O            1   0.704   0.420  m1/y1 (tout_OBUF)
     OBUF:I->O                 3.272          tout_OBUF (tout)
    ----------------------------------------
    Total                      6.209ns (5.194ns logic, 1.015ns route)
                                       (83.7% logic, 16.3% route)
```

Figure.8. Existing Method delay

```
-------------------------------------------------------------------------
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 2 / 2
-------------------------------------------------------------------------
Offset:              4.283ns (Levels of Logic = 1)
  Source:            test_fail (FF)
  Destination:       test_fail (PAD)
  Source Clock:      clk rising

  Data Path: test_fail to test_fail
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q              1   0.591   0.420  test_fail (test_fail_OBUF)
     OBUF:I->O                 3.272          test_fail_OBUF (test_fail)
    ----------------------------------------
    Total                      4.283ns (3.863ns logic, 0.420ns route)
                                       (90.2% logic, 9.8% route)
```

Figure.9. Proposed Method delay

V.CONCLUSION

The proposed approach is a new low power pattern generation technique is implemented using a modified conventional LFSR. Comparisons of the number of test patterns (NP) required to hit target fault coverage (FC), the average and peak power of LT-LFSR, LPATPG and modified clock scheme. The used 50 different seeds for 10 different polynomials in the experiment. The performance of LT-LFSR is seed and polynomia l-independent. The required number of patterns provides target FC does not quadruples, and preserving randomness. By using this low transition test pattern generator using LFSR for Test Pattern Generation (TPG) technique we conclude that power dissipation is reduced during testing. The transition is reduced by increasing the correlation between the successive bits, reduces the average and peak power of a circuit during the test mode. By increasing the correlation between the test patterns in the CUT and eventually the power consumption is reduced. Additional intermediate test patterns inserted between the original random patterns reduces the PI activities, average and peak power of combinational and sequential circuits during the test mode with do not effect on FC.

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