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An Area Efficient, Power Reduced and Speed Improved Serial Type Daisy Chain Memory Register Using Pulsed Latch

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Abstract:
This paper proposes an area and power efficient shift register using pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals. The area and power consumption are reduced by replacing flip-flops with pulsed latches. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A shift register of 256-bit using pulsed latches with VDD=1.8V was fabricated using a 0.18ìm CMOS process. At a 100 MHz clock frequency the power consumption is 1.2mW. The core area is 6600ìm2. The shift register using digital pulsed latches will saves 44% power and 37% area 44% power compared to the conventional shift register with flip-flops. Shift registers can be used as simple delay circuits. Several bidirectional shift registers could also be connected in parallel for a hardware implementation.

Keywords: shift register, flip-flop, pulsed clock, bit array, pulsed latch

I. INTRODUCTION

In a digital circuit design, flip-flops are widely used as the clock tree branch elements. They are used to sample and store the branch data and send to the next stage combinational circuit when the next clock edge is arrived. In a high performance application, pipeline technique is widely used to increase the clock frequency and throughput rate. Therefore, the flip-flop consumes great part of power and occupies a larger area in a digital system. The traditional flip-flop is master slave flip-flop. It is composed with two latches which are triggered at opposite clock edge. When the master latch is activated in the sample data state, the slave latch keeps the data and sends data to the stage. Similarly, when the slave latch is activated in the sample data state, The master latch keeps data and sends data to the slave latch. The pulsed latch is proposed to replace master-slave flip-flop to increase the system performance. It uses a pulse generator to generate a short pulse and activates the latch with the pulse. It could make the latch to work as a flip-flop. The advantage of pulsed latch is the faster setup time and soft-clock edge property. In recent years, there has been an increasing demand for high-speed digital circuits at low power consumption. The double edge triggered (DET) flip-flop has been paid much attention. The DET could maintain the same throughput rate at half clock frequency comparing with conventional single edge triggered flip-flop.

Latches are transparent while the internal memory is being set from the data input and the possible changes of the input value can be transmitted to the output.

Flip-flops are not transparent; reading the input value and changing the flip-flop's output are two separate events.

II. LITERATURE REVIEW

Shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4Kbitshift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bitshift register. A 16 mega-pixel CMOS image sensor uses a 45K-bit shift register.

As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register.

The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

III. PROPOSED SHIFT REGISTER

A master-slave flip-flop using two latches can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of

the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low-power consumption. The pulsed latch cannot be used in shift registers due to the timing problem. The shift register in consists of several latches and a pulsed clock signal (CLK pulse). The operation waveforms show the timing problem in the shift register.

The output signal of the first latch (Q1) changes correctly because the inputs signal of the first latch (IN) is constant during the clock pulse width. But the second latch has an un-certain output signal (Q2) because its input signal (Q1) changes during the clock pulse width. One solution for the timing problem is to add delay circuits between latches. The pulsed latch cannot be used in shift registers due to the timing problem. The shift register in consists of several latches and a pulsed clock signal (CLK pulse).

Input signal of the latch is delayed and reaches the next latch after the clock pulse. The output signals of the first and second latches (Q1 and Q2) change during the clock pulse width, but the input signals of the second and third latches (D2and D3) become the same as the output signals of the first and second latches (Q1 andQ2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. How- ever, the delay circuits cause large area and power over heads.

The operation waveforms show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signals of the first latch (IN) is constant during the clock pulse width. But the second latch has an un-certain output signal (Q2) because its input signal(Q1) changes during the clock pulse width. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. How- ever, the delay circuits cause large area and power over heads. Another solution is to use multiple non-overlaps delayed pulsed clock signals. The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch.

Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. The proposed shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK pulse<1 : 4>and CLK pulse <T>).

In the 4-bit sub shift register#1, four latches store 4-bit data(Q1-Q4) and the last latch stores1-bit temporary data (T1) which will be stored in the first latch(Q5) of the 4-bit sub shift register#2. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator. The sequence of the pulsed clock signals is in the opposite order of the five latches. Initially, the pulsed clock signal CLK pulse<T> updates the latch data T1 from Q4.

And then, the pulsed clock signals CLK pulse<1:4> update the four latch data from Q4 to Q1sequentially. The latches Q2–Q4 receive data from their previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN).The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop.

The pulsed latch is an attractive solution for small area and low-power consumption. But the second latch has an un-certain output signal (Q2) because its input signal (Q1) changes during the clock pulse width. One solution for the timing problem is to add delay circuits between latches. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

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Each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. When an N-bit shift register is divided into K-bit sub shift registers. The number of clock pulse circuits is K+1 and the number of latches is N+N/K. A K-bit sub shift register consisting of K+1 latch requires K+1 pulsed clock signals. The number of sub shift registers (M) becomes N/K, each sub shift register has a temporary storage latch. Therefore, N/K latches are added for the temporary storage latches

IV. METHOD OF IMPLEMENTATION

The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop.

The proposed shift register uses latches instead of flip-flops to reduce the area and power consumption. In chip implementation, the SSASPL (static differential sense amp shared pulse latch) in Fig.8, which is the smallest latch, is selected. The original SSASPL with 9 transistors is modified to the SSASPL with 7transistors by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch.

The SSASPL uses the smallest number of transistors (7transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal. The SSASPL updates the data with three NMOS transistors and it holds the data with four transistors in two cross-coupled inverters. It requires two differential data inputs (D and Db) and a pulsed clock signal. When the pulsed clock signal is high, its data is updated. The node or Qb is pulled down to ground according to the input data (D and Db). The pull-down current of the NMOS transistors must be larger than the pull-up current of the PMOS transistors in the inverters.

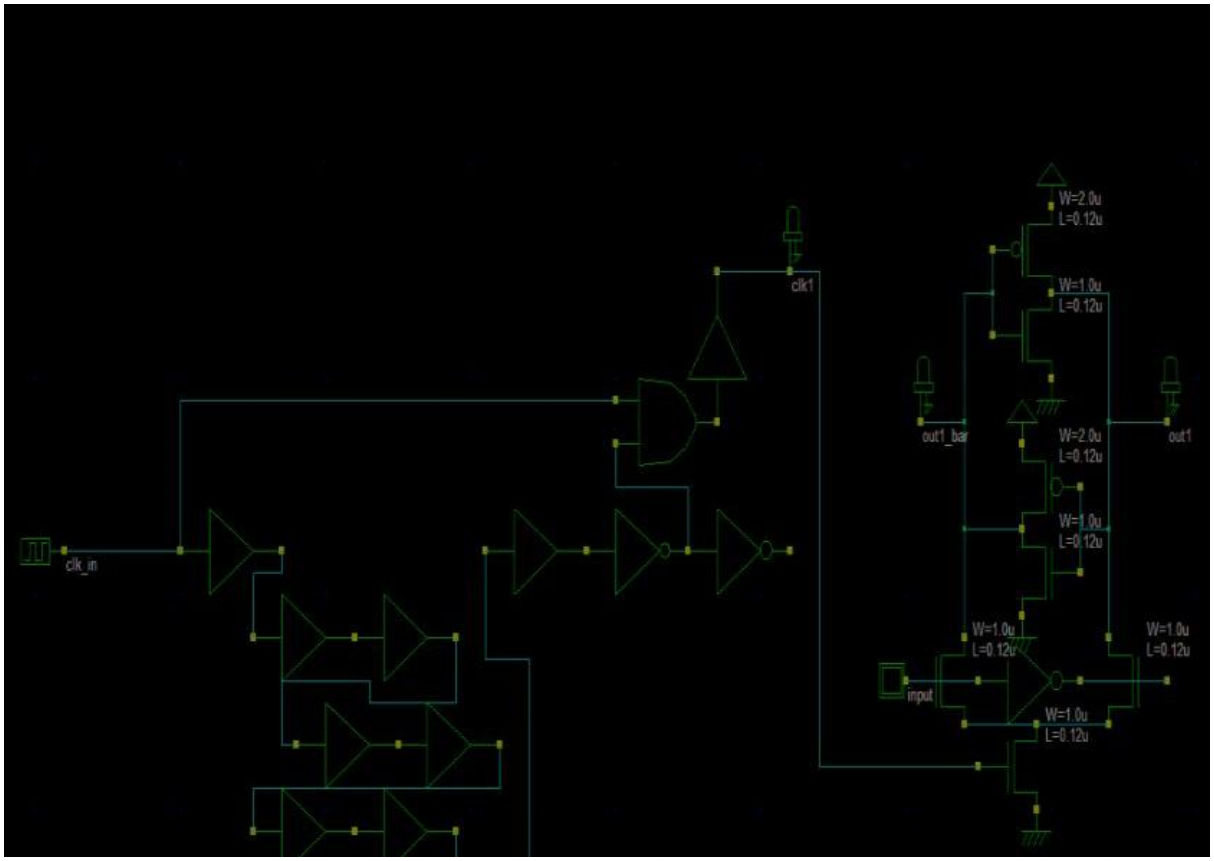

Figure.1. Schematic Of SSASPL Pulsed Latch Driven By Pulsed Clock Signal.

The figure shown explains the SSASPL with pulsed clock signal. In chip implementation, the SSASPL (static differential sense amp shared pulse latch) in Fig.8, which is the smallest latch, is selected. The original SSASPL with 9 transistors is modified to the SSASPL with 7 transistors by removing an inverter to generate the complementary data input (Db) from the data input(D). The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flip-flops to reduce the area and power consumption. In chip implementation, the SSASPL (static differential sense amp shared pulse latch),

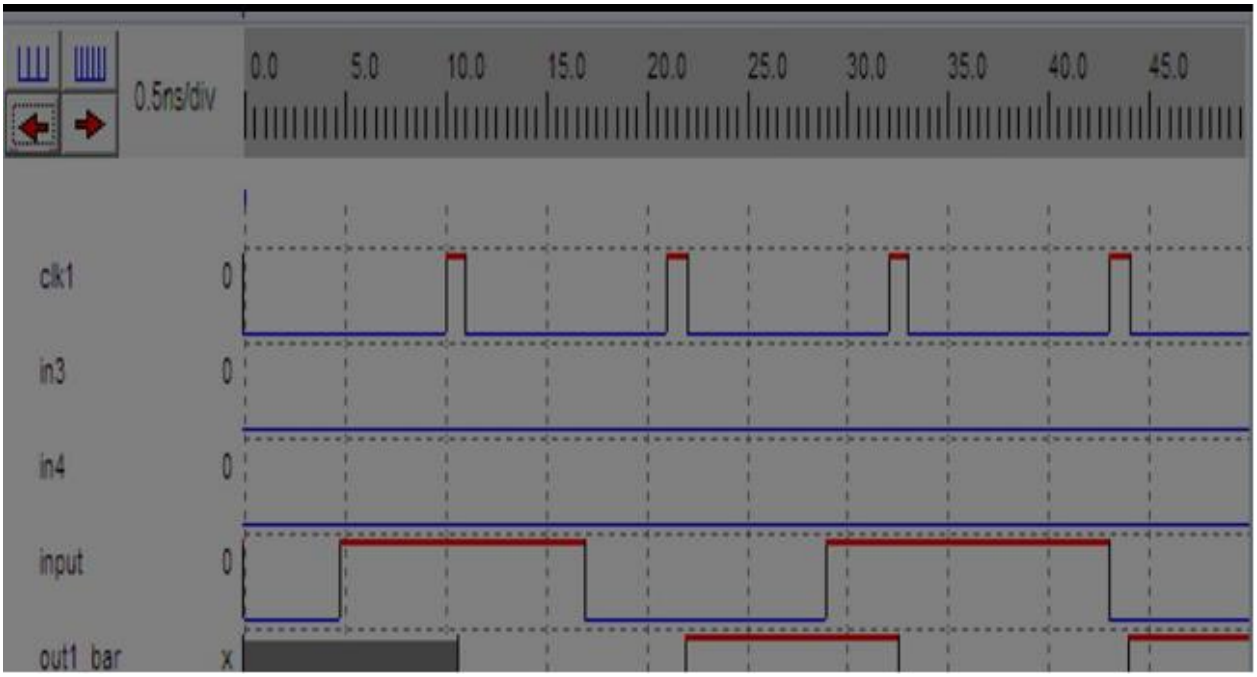

Figure.2.Simulation Of SSASPL Pulsed Latch Driven By Pulsed Clock Signal.

The figure shows the simulation waveforms of a shift register with the SSASPLs driven by the delayed pulsed clock signals. This example has three shift registers (Q1–pulsed clock delay is 220 ps by adding the pulse interval of 50 ps between clock pulses to the clock pulse width of 170 ps. The sequence of the pulsed clock signals is in the opposite order of the latches. Each latch has a constant input during its clock pulse so there is no timing problem.

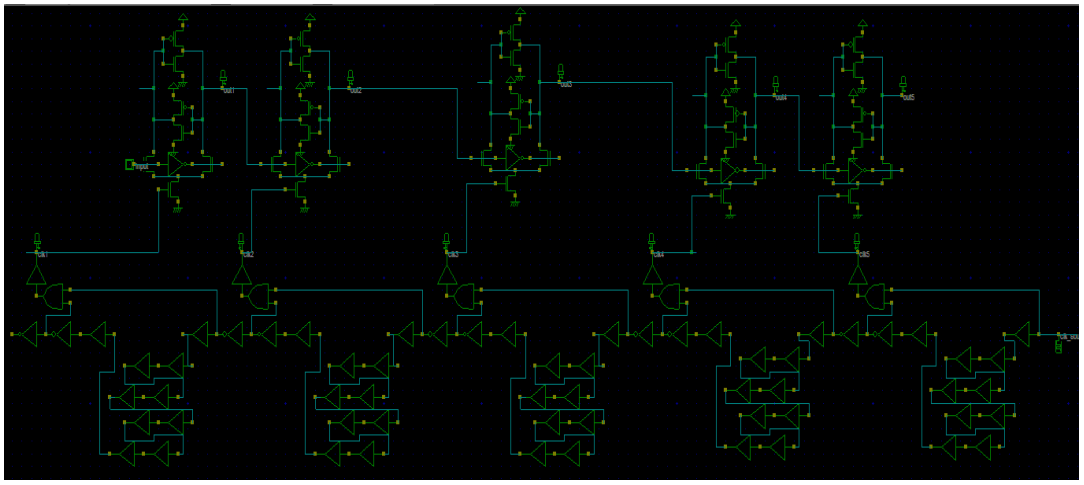

Figure.3. Schematic of Shift Register with SSASPL Pulsed Latch Driven Delayed Pulsed Clock Signal

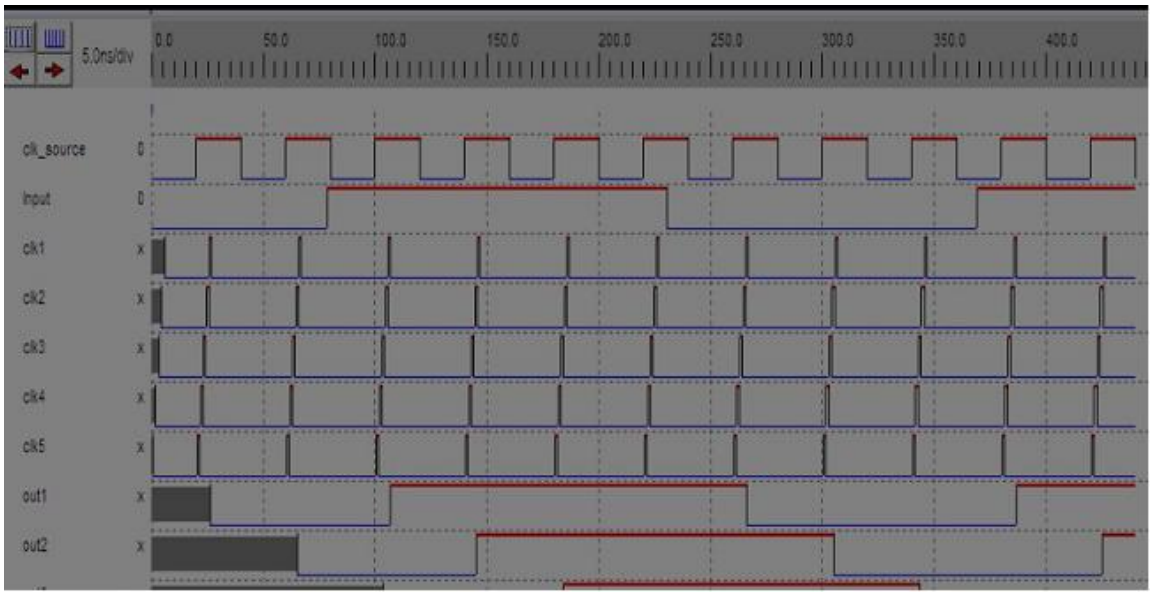

Figure.4. Simulation Waveforms Of Shift Register With SSASPL Pulsed Latches Driven By Delayed Pulsed Clock Signals.

V. PERFORMANCE COMPARISON

Table I show the transistor comparison of pulsed latches and flip-flops. The transmission gate pulsed latch (TGPL) [7], hybrid latch flip-flop (HLFF) [8],conditional push-pull pulsed latch (CP3L) [9], Power-PC-style flip-flop (PPCFF)[10], Strong-ARM flip-flop (SAFF) [11], data mapping flip-flop (DMFF) [12],conditional pre-charge sense-amplifier flip-flop (CPSAFF) [13], conditional capture flip-flop (CCFF) [14], adaptive-coupling flip-flop (ACFF) [15] are compared with the SSASPL [6] used in the proposed shift-register. When counting the total number of transistors in pulsed latches and flip-flops, the transistors for generating the differential clock signals and pulsed clock signals are not included because they are shared in all latches and flip-flops.

The SSASPL uses 7transistors, which is the smallest number of transistors among the pulsed latches [6]–[9]. The PPCFF uses 16 transistors, which is the smallest number of transistors among the flip-flops [10]–[15].The total area of the N flip-flops and clock buffer for the N conventional shift register is N x α, where α is the total area of a flip-flop and a unit clock buffer for driving a flip-flop. The total area of N (1+1/K) latches and a clock buffer for the N-bit proposed shift register is N (1+1/K) x β, where β is the total area of a latch and a unit clock buffer for driving a latch. The area of K+1 clock-pulse circuits is (K+1) x γ, Where γ is the area of a clock-pulse circuit.

As N increases, the area ratio is reduced to β/α x (1+1/K), as shown in Fig. β is 48.7%
From the circuit layouts. When and N = 4096 and K = 16, the area ratio is 52.2%. As
N increases, the area ratio is reduced to 51.7% for K = 16

VI. CONCLUSION

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. The small number of pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 4 –bit shift register using pulsed latches is implemented and simulated on Micro-wind environment.

VII. FUTURE SCOPE

SRAM is a type of semiconductor memory which is volatile in nature (retains the data as long as power is being supplied).It performs both read and writes operations to store and fetch the data, based on the particular address. The read and write operations are controlled by the word line. Based on the bit line condition the data in it is stored and consists of a 1bit latch to

store the data The 256bit pulsed latch shift register is used as part of SRAM in order to store the data in SRAM and fetch the data according to the given address location. So that it has low power consumption than the memory with general latch.

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