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Design of Low Power and High Performance of a Novel 13T SRAM for Ultra Low Power Applications

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Abstract:
The most vulnerable of these circuits are memory arrays that cover large areas of the silicon die and often store critical data. Radiation hardening of embedded memory blocks is commonly achieved by implementing extremely large bit cells or redundant arrays and maintaining a relatively high operating voltage. However, in addition to the resulting area overhead, this often limits the minimum operating voltage of the entire system leading to significant power consumption. In this paper, we propose the first radiation-hardened static random access memory (SRAM) bit cell targeted at low-voltage functionality, while maintaining high soft-error robustness. The proposed A novel sleep techniques was at circuit level for the reduction of power consumption, delay and leakage.

Keywords: Sleep, Dual Sleep, static random access memory (SRAM).

1. INTRODUCTION

Exploitation of very large scale integration (VLSI) technology has developed to the point where millions of transistor can be implemented on a single chip. Complementary metal oxide semiconductor (CMOS) has been the backbone in mixed signal because it reducing power and providing good mix component for analog and digital design. Power consumption is one of the top issues of VLSI circuit design, for which CMOS is the primary technology. Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before the mobile era, power consumption has been a fundamental problem. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay and area and thus, designers are required to choose appropriate techniques that satisfy application and product needs. In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor. when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limits the application of each technique. We propose a new approach, thus providing a new choice to low leakage power VLSI designers.

2. LITERATURE SURVEY: Power dissipation is one of the most important aspects of current nano scale VLSI design. Ultra low power (ULP) operation is of particular importance in VLSI chips for space applications, where available energy resources are limited. Future small, low-cost satellites have an even lower power budget, as the total satellite weight is often reduced by restricting the use of heavy batteries and power supplies. The most efficient way to achieve ULP operation in integrated circuits is to aggressively reduce the supply voltage (V***DD***) and operate all components of the chip in the near-threshold or sub threshold region thereby significantly reducing both static and dynamic power consumption. However, in addition to the well-known challenges of a low-voltage circuit design, such as increased delay, sensitivity to process variations, and temperature fluctuations, low-voltage circuits are much more susceptible to radiation effects than circuits powered at nominal supply voltages.

3. CIRCUIT DESIGN

A.13TSRAM BITCELL:

Bit cell Design SRAM design for low-voltage operation has become increasingly popular in the recent past. Various bit cell designs and architectural techniques have been proposed to enable operation deep into the sub threshold region. These designs generally incorporate the addition of a number of transistors into the bit cell topology, compared with the baseline 6T SRAM bit cell, trading off density with robust, low-voltage functionality. However, these bit cells were designed for operation under standard operating environments, and thereby, does not provide sufficient robustness to SEUs under high-radiation conditions. In addition, the design architecture of these cells is based on the standard 6T cell. Therefore, the 6T cell has the same hardening ability to most, if not all, these unprotected cells. Especially when compared with radiation hardening solution designs. The bit cell is specifically designed to enable robust, low-voltage, ULP operation in space applications and other high-radiation environments. This is achieved by employing a dual-feedback, separated-feedback mechanism to

overcome the increased vulnerability due to supply voltage scaling. The schematic representation of the 13T bit cell. The storage mechanism of this circuit comprises five separate nodes: *Q*, *QB*1, *QB*2, *A*, and *B*, with the acute data value stored at *Q*. This node is driven by a pair of CMOS inverters made up of transistors N3, P3, N4, and P4 that are, respectively, driven by the inverted data level, stored at *QB*1 and *QB*2. *QB*1 and *QB*2 are, respectively, driven to *V*DD or GND through devices P1, P2, N1, and N2 that are controlled by the weak feedback nodes *A* and *B* that are connected to *Q* through a pair of complementary devices (P5 and N5) gated by *QB*2. By driving the acute data level by a pair of equipotent ally driven, but independent, inverters, a strong, dual-driven feedback mechanism is applied with node separation for SEU protection. This setup effectively protects *Q* from an upset, while achieving a high critical charge at node *Q*.

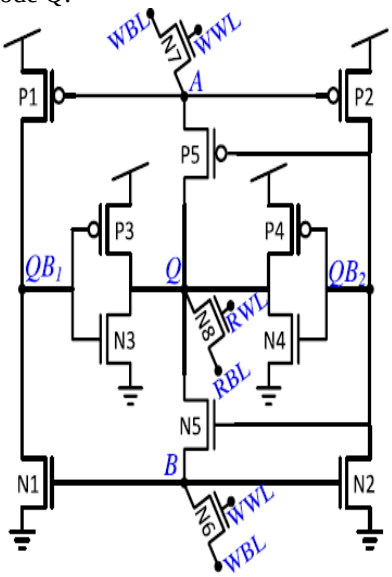

Figure.1. Schematic Of The 13t Sram

B.DUAL SLEEP:

However, area requirement is max for this technique since every transistor is replaced by three transistors. Dual sleep Technique is (Fig:2) uses the advantage of using the two extra pull- up & pull-down transistors in sleep mode either in OFF/ON state. To all logic circuitry the dual sleep portion is designed as common. For a certain logic circuit less number of transistors are enough to apply

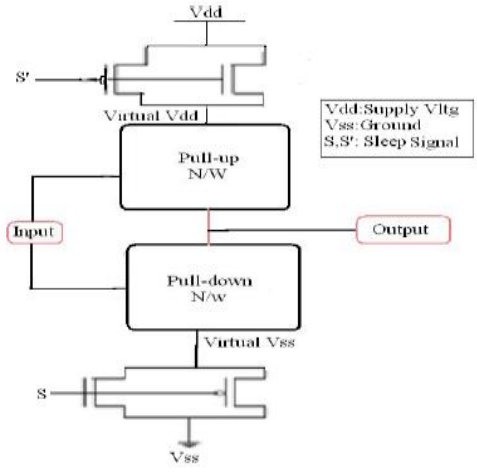

Figure.2. Dual Sleep

C.SLEEP TECHNIQUE:

The most well-known traditional approach is the sleep approach .In the sleep approach, both(i) an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and Gnd

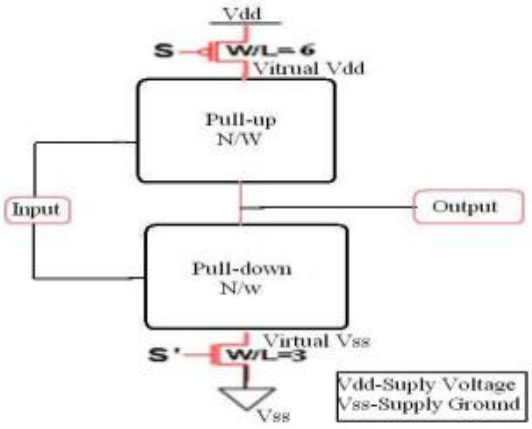

Figure.3. Proposed Sleep Method

4. SIMULATIONS AND RESULTS

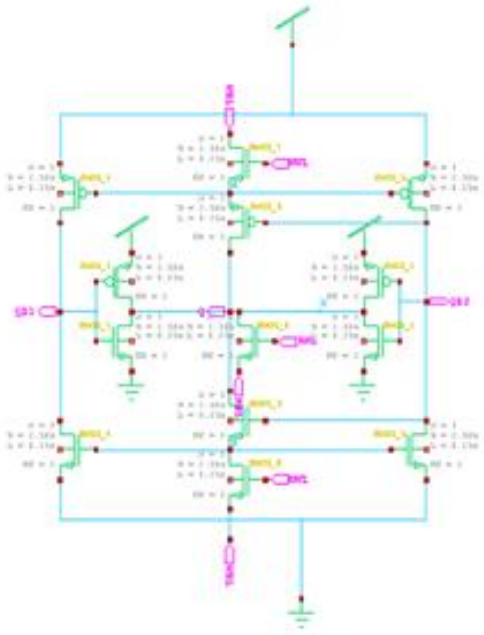

Figure.4. Schematic Of The 13t Sram

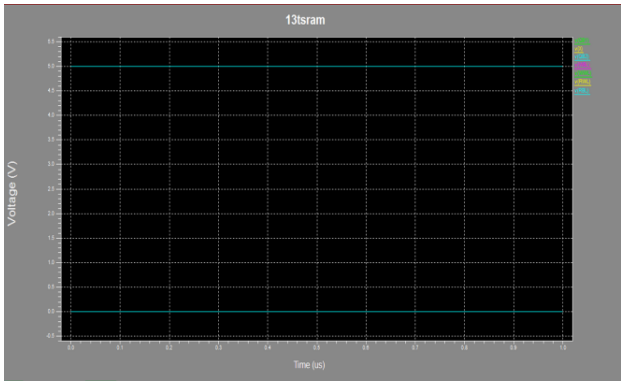

Figure.5. Waveform of 13tsram

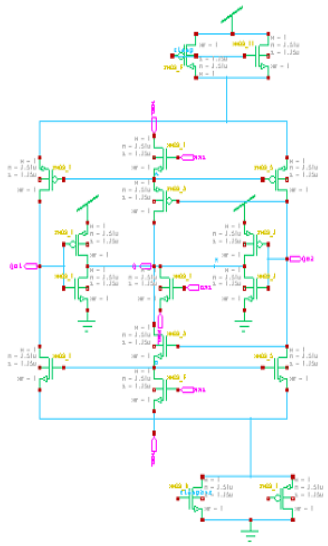

Figure.6. Schematic of Dual Sleep

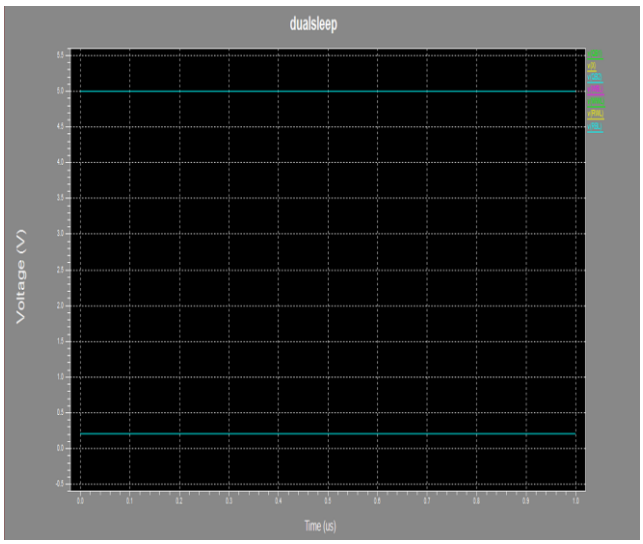

Figure.7. Waveform Of Dual Sleep

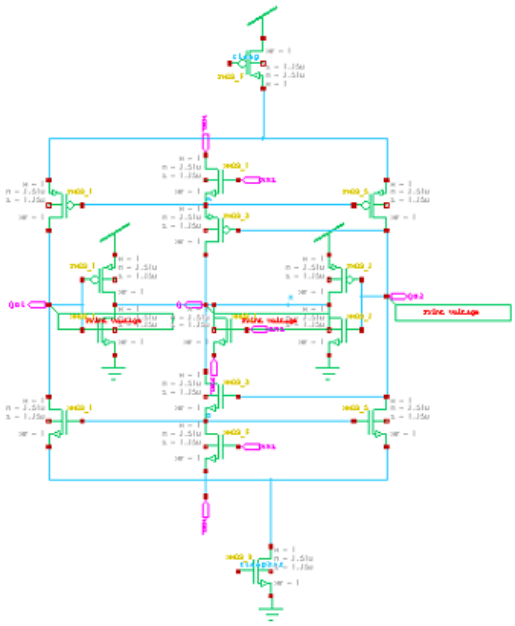

Figure.8. Schematic of Sleep

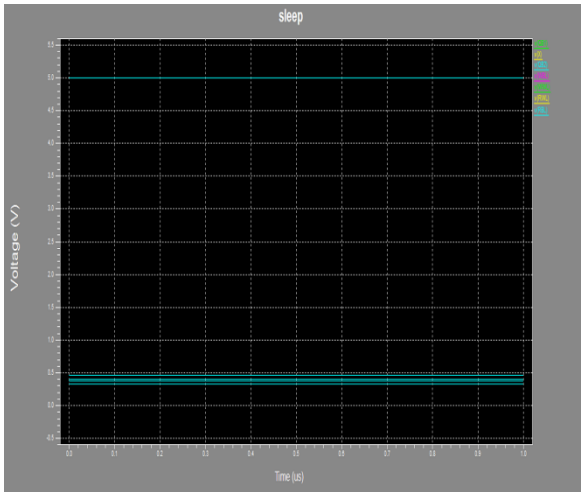

Figure.9. Waveform of Sleep

Table.1. Comparison B/W Proposed Method and Other Techniques

S.NO	TYPE	POWER	DELAY	POWER DELAY PRODUCTS(PDP)	TEMPARATURE	TEM POWER	TEM DELAY
1	13T SRAM	2.113340e-005 walts	5.48E-10	1.1577510522e-14w	0	5.897575e-005w	9.42E-10
					20	2.136940e-005w	5.43E-10
					40	2.025949e-005w	5.62E-10
					80	1.753738e-005w	6.59E-10
2	SLEEP	4.279824e-006walts	1.50E-07	6.4052322912e-13w	0	4.019371e-006w	1.50E-07
					20	4.231812e-006w	1.50E-07
					40	4.412625e-006w	1.50E-07
					80	9.787436e-006w	1.50E-07
3	DUAL SLEEP	3.211388e-005walts	5.00E-08	1.607235466624e-12w	0	2.229747e-005w	5.00E-08
					20	2.496031e-005w	5.00E-08
					40	1.914617e-005w	5.00E-08
					80	1.903571e-006w	5.00E-08

5. CONCLUSION:

Sub threshold leakage power consumption is a great challenge in nano-meter scale (CMOS) technology, although previous techniques are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, based upon technology & design criteria the designers can choose the techniques. In this paper, we provide novel circuit structure in terms of static & dynamic powers named as “sleep method” it’s a new remedy for designers. This technique shows the least speed power product among all techniques. The Proposed technique achieving ultra-low leakage power consumption with much less speed, especially it shows nearly 50-60% of power than the existing. So, it can be used for . future IC'S for area & power Efficiency

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