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A Review on Half Subtractor at Transistor Level

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Abstract:
Integrated circuit is a circuit where passive and active components can be implemented on a chip. Initially an IC could accommodate only few components but now days we can fabricate billions of components on a single IC. Half subtractor is using for subtracting the numbers. In this paper discuss about designing and technologies of half subtractor

Keywords: CMOS, VLSI, XOR, AND, QCA, DSP

I. INTRODUCTION

A low-power combination need can be defined at different design levels, such as the circuit design and the process technology level. As the modern multimedia world is developing low power devices are in demand [1].Digital circuits which are designed by using conventional CMOS cannot fulfill these basic requirements so some solutions are found out and the outcome has resulted in the form of pass transistor logic [2]. In VLSI designing the rapid increase in demand for low power can be dealt at various logic levels, such as circuit, architectural and layout. At circuit design level substantial quantity of power can be saved by way of proper option of a logic manner. The proper option of a logic manner is value able because all significant constraints leading power dissipation, switching capacitance, transition motion, and short circuit currents are strongly prejudiced by the chosen logic style [3]. Indeed, designing high-speed low-power circuits with CMOS technology has been a main research problem. Numerous logic families have been planned and used to recover circuit routine outside that of conventional static CMOS family. In addition, due to technology growing the number of transistors on chip, the presentation of static CMOS circuits originates at considerable area where power dissipation value that may be critical, specifically for transportable appliances. Innovative devices that address the power and performance encounters must be therefore, explored [4]. There are a various logic methods through which a circuit can be realized. The proper choice of a logic strategy is significant because all important constraints governing power dissipation-switching capacitance, transition activity, and short circuit currents are powerfully prejudiced by the chosen logic design [5].

II. HALF SUBTRACTOR

A subtractor performs subtraction which is one of the four basic binary operations. In many computers and other kinds of processors, subtractors are used not only for the arithmetic calculations, but are also frequently used in other parts of the processor. The subtractors can be constructed to operate on binary numbers. Depending upon the application of the device or the purpose of the application to be performed, the inputs to the circuit device may vary from two to three. We could possibly use a Half-Subtractor if we have two inputs while for three inputs, a Full-Subtractor can be used. Subtractor is a combinational circuit which represents the smallest unit for subtraction in digital systems. It is not only used for arithmetic calculation in many device processors but also used in other part of processor for calculating address. Stack pointer use subtraction operation in push-pop logical operation for storage of address. The simplest combinational circuit which performs the arithmetic subtraction of two binary digits is called half-Subtractor [1]. This is the necessary building block for designing a VLSI system.Figure1.1 shows the logic diagram of half subtractor. In which, two inputs A and B are applied at the different Gates and corresponding output are gotted. These are the two inputs which consist of two 1-bit numbers A and B, where A represents Minuend and B represents Subtrahend. From the logic symbol, there are two outputs corresponding inputs. Those outputs are the Difference (D) of A and B and Borrow bit denoted by Bout.

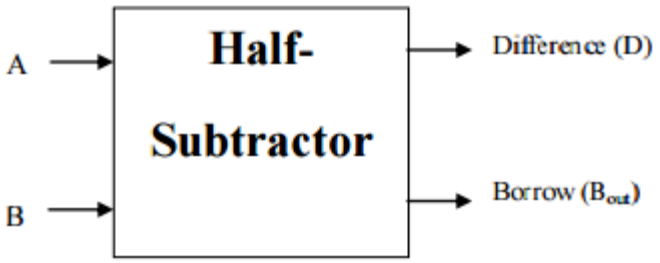

Figure.1. Logic Symbol of half Subtractor

1 Bit Half Subtractor

A conventional Half-subtractor circuit is a combinational circuit that can be used to subtract one binary digit from another to produce a Difference output and a Borrow output. Functionally, the half subtractor consists of a 2 input XOR Gate, an INVERTER and a 2 input AND gate .The Borrow output here specifies whether a „1" has been borrowed to perform the subtraction. The Half-Subtractor at the gate-level and truth table are shown in Fig 1.1 and Table 1.1.

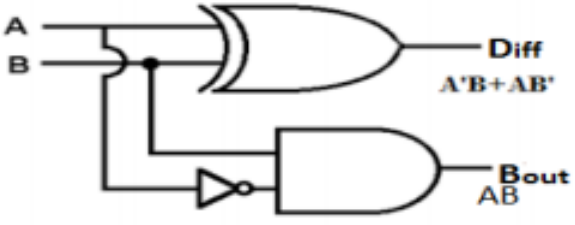

Figure.2. Gate Level 1 bit Conventional Half Subtractor.

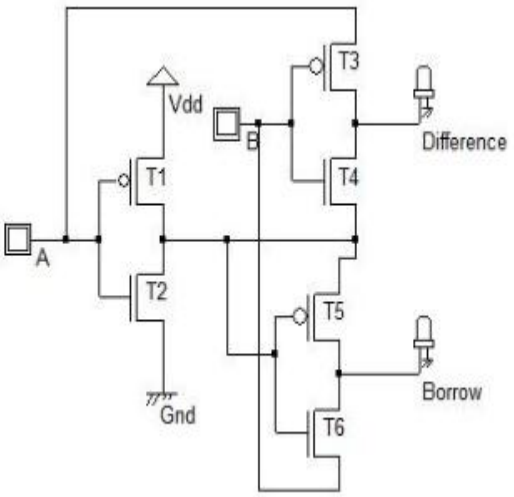

Figure.3. Circuit diagram of Conventional Half Subtractor

Table.1. Truth Table of 1 bit half subtractor.

A	**B**	B_{out}	Diff
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The Boolean expression for the two output variables are given by the equations.

Diff = A'B + AB'

B_{out} = A'B

III. LITERATURE REVIEW

The designing of low power systems has emerged as one of the vital theme of electronic industries due to the point that, power consumption is drawing much of the absorption in any very large scale integration (VLSI) chip design. Design of low power circuit for high performance is the necessary main concern of VLSI technique. This paper presents designing of Half Subtractor using basic gates which are drawn by conventional CMOS and Pass Transistor Logics based on 45nm technology. In comparison between the conventional CMOS half subtractor and using Pass Transistor Logic the delay is 10.5% less in PTL‟s half subtractor which is due to less number of transistors used in Pass Transistor Logic which in further has reduced the transistor count to 28.57% [1]. In digital signal processing (DSP), image processing and performing arithmetic operations in microprocessors substractor plays an important role. In this paper, a 2-bit half subtractor circuit has been designed and analyzed. A comparative study has been done in account of the silicon area and the power consumption in the designed circuit using different channel lengths such as 65nm, 45nm and 32nm. The designed circuit has shown a remarkable reduction in the consumed power of 84.64% and a reduction of 67.08% in consumed area in 32nm foundry as compared to 65nm CMOS foundry [3]. The necessity of achieving zero power dissipation in low power digital design yields the interest in the invention of Reversible logic gate which plays essential role in the modern computing. The optical implementation of reversible logic gate based on Semiconductor Optical Amplifier based Mach-Zehnder Interferometer sets the paradigm for the model ‘Optical Signal Processing’. The proposed reversible logic gate named NR (Naveen Raymond) is designed to implement Half adder and Half subtractor, similarly a couple of NR Gates are used to realize Full adder and Full subtractor. The Circuits are simulated using the Opt system Software and the output is verified [2]. Quantum Dot cellular Automata (QCA) is an emerging, promising alternative to CMOS technology that performs its task by encoding binary information on electronic charge configuration of a cell. All circuit based on QCA has an advantages of high speed, high parallel processing, high integrity and low power consumption. Reversible logic gates are the leading part in Quantum Dot cellular Automata. Reversible logic gates have an extensive feature that does not lose information. In this paper, we present a novel architecture of half subtractor gate design by reversible Feynman gate. This circuit is designed based on QCA logic gates such as QCA majority voter gate, majority AND gate, majority OR gate and inverter gate. This circuit will provide an effective working efficiency on computational units of the digital circuit system [4]. In this paper we are presenting a Half-Subtractor using Adaptive Voltage Level (AVL) technique consuming less power than the conventional one .The main objective is to design that half subtractor using either of the two adaptive voltage level(AVL) techniques to reduce the sub threshold leakage current which plays a very important role in the reduction of power dissipation. We can bring down the value of total power dissipation by applying the AVLG (adaptive voltage level at ground) technology in which the ground potential is increased and AVLS (adaptive voltage level at supply) in which supply potential is raised. Also the reduced transistor count add to the further lowering of power consumption of the realized Half-Subtractor circuit which is optimized at .90 micron technology using AVL technique. The AVL technique based Half-Subtractor compared to conventional one based on power consumption, speed, layout area and propagation delay is more preferred. The circuit is simulated on micro wind and DSCH in. 90 micron CMOS technology [6]. Arithmetic circuits play a vital role in designing of any VLSI system. Subtractor is one of them. In this paper, Half-Subtractor is being designed using Adaptive Voltage Level (AVL) techniques. This design consumed less power as compare to conventional design. We can reduce the value of total power dissipation by applying the AVLG (adaptive voltage level at ground) technology in which the ground potential is raised and AVLS (adaptive voltage level at supply) in which supply potential is increased. This paper represents how to control power using AVL techniques. The AVL technique based Half-Subtractor compared to conventional design that based on power consumption, propagation delay, speed and layout area is more preferred. Power consumption of the proposed cell is measured and compared. The result shows that there is a significant reduction in power consumption for this proposed cell with the AVL technique. This design is much useful in designing the system that consumed less power. The circuit is simulated on MicroWind 3.1 and DSCH in 65 nanometer CMOS technology [5].

IV. CONCLUSION

A new better design can be designed in future that will provide better parameters with less area. Area can be further reduced by decreasing the number of transistors. Another method is that lower technologies can be used for further improvement. Frequency can be increased to get high switching activity of the transistors. Power delay product can be reduced by just reducing the power and delay for the circuit by controlling the width of transistor. The circuit can be changed by using the different designs. Modification can be done by combining all

these factors together for better results.

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