



Design of a Multiplier using Low Power High Speed Hybrid Full Adder

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Abstract:

In this paper, a hybrid 1-bit full adder design employing both Pass Transistor Logic (PTL) and transmission gate (TG) logic is reported. The circuit was implemented using Cadence Virtuoso tools in 180nm technology. Performance parameters such as power and delay were compared with the existing designs such as complementary pass-transistor logic, transmission gate adder, transmission function adder, hybrid full adder. For 1.8-V supply at 180-nm technology, the average power consumption and delay of the proposed adder was found to be 26.68 μ W and 3.55ps. The design was further implementing on 2*2 Braun multiplier. When compared with the present full adder styles, this implementation was found to supply vital improvement in terms of power and speed.

Index terms: Braun multiplier, highspeed, hybrid design, lowpower.

I. INTRODUCTION

Increased usage of battery operated transportable devices like cellular phones, personal digital assistants (PDAs), and notebooks demand VLSI, associated ultra large scale integration style with an improved power delay characteristics. Full adders are the essential building block of these devices Different logic designs is accustomed to design a 1-bit full adder cell. Design is broadly classified into two categories, they are:1) static vogue and 2) dynamic vogue. Static full adders usually has lot of reliability, less complicated with less power demand, however the on chip space demand is sometimes larger compared with its dynamic counterpart. Different logic style tends to offer one performance facet at the expense of others. Standard static Complementary Metal–Oxide–Semiconductor (CMOS), dynamic CMOS logic, complementary pass-transistor logic (CPL) and transmission Gate Full Adder (TGA) are the foremost vital logic style design within the standard domain. The combination of any two logic design is called as Hybrid logic style. This style exploits the options of various logic designs to boost the performance of the adder [1]. Each logic style has its own advantages and disadvantages. Standard static CMOS full adder is based on regular CMOS structure with pull-up and pull-down transistors, this adder provides full output voltage swing against voltage and transistor sizing. The limitations of this design are its lager area and slower speed due to the availability of PMOS devices and larger input capacitance of the static CMOS logic gates. Complementary Pass Transistor (CPL) is fast and provides full voltage swing output. CPL adder requires 32 transistors but it has larger power consumption because of the presence of static inverter and lot of internal nodes. Another logic style of designing an adder is hybrid logic style. These adders are designed with the combination of more than one logic style to enhance the overall performance of the system. The main focus of the hybrid logic style is to reduce the number of transistors and power dissipation nodes of the adder cell [2].

II. COMPARATIVE ANALYSIS OF DIFFERENT TYPES OF FULL ADDER CIRCUITS

Several logic designs reutilized in the past to design a full adder cell. Every logic style has its own benefits and bottlenecks.

A. Conventional CMOS Full Adder

A classical design of standard static CMOS full adder relies on regular CMOS structure with pull-up and pull-down transistors. Complementary transistor pairs build the circuit layout easy. CCMOS generates carry through a static gate. The benefits of using CCMOS is that it's layout regularity, high noise margin and stability at low voltage attributable to complementary transistor pair and smaller number of interconnecting wires. The disadvantages is that it uses c_{out} signals to generate sum which produces an unwanted extra delay. It has weak output driving capability due to series transistor in output stage and consumes additional power and huge silicon area. The circuit is shown in Fig.1

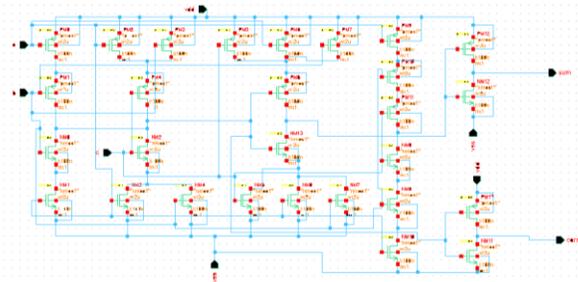


Figure.1. CCMOS schematic diagram

B. Complementary Pass Transistor Logic

The basic difference between the Pass Transistor Logic (PTL) and Complementary CMOS logic style is the source side of the pass transistor logic network is connected to some input signal instead of power lines. It uses 32 transistors which is shown in

Fig. 2.CPL provides many intermediates nodes and their complements to make the outputs. By using PTL, number of transistors can be reduced. When the transistor gates are oversized, the input overloading occurs and creates high capacitances values. This problem occurs in CPL and CMOS. PTL has an intrinsic problem which is threshold voltage drop so, output inverters are necessary to guarantee the drive ability. CPL is not appropriate choice for low power due to its high switching activity of intermediate nodes, high transistor count, its static inverters and overloading of its inputs.

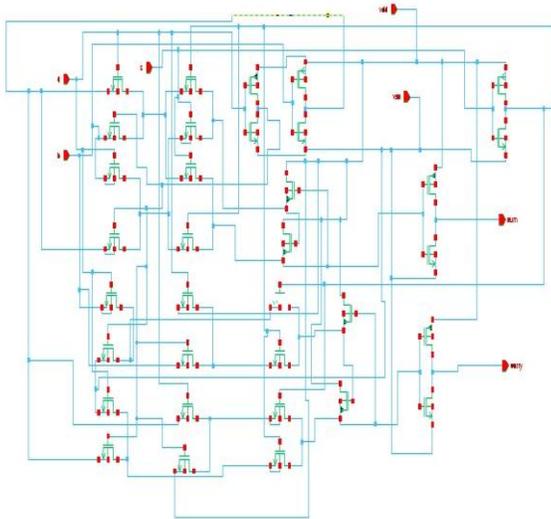


Figure. 2. CPL schematic diagram

C. Transmission Full Adder

TFA is based on transmission function theory. TFA consists of 16 transistors as shown in Fig. 3. This circuit uses both nmos and pmos transistors. There is no voltage drop problem but it requires double the number of transistors to design the function.

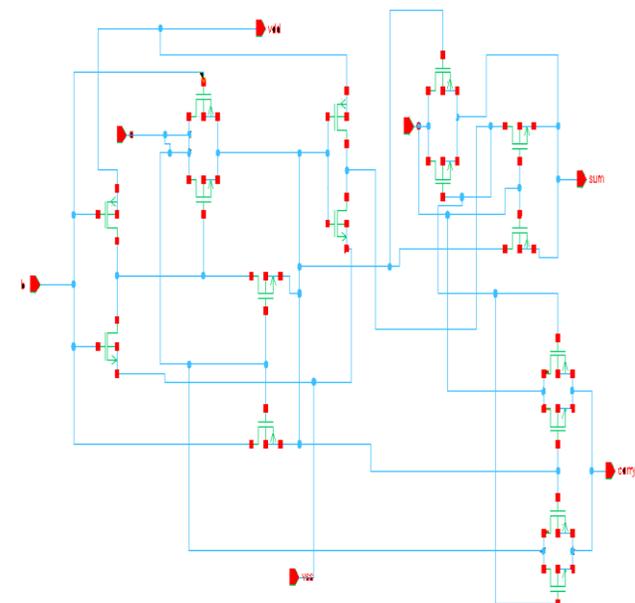


Figure.3. TFA schematic diagram

D. Hybrid Full Adder

Based on both PTL and TG circuit design techniques hybrid full adder is implemented as shown in Fig. 4. Hybrid full adder is

composed of three logic architecture modules including XOR-XNOR module, Sum module and Carry module. The XOR – XNOR module performs XOR and XNOR operations on input A and B, and then both the XOR XNOR outputs signals used to drive sum and carry module to produce sum and carry output. Due to adopting both the XOR-XNOR module and carry module the transistor count for hybrid full adder can be reduced to 16. As a result the circuit complexity of hybrid full adder is simplified [3].

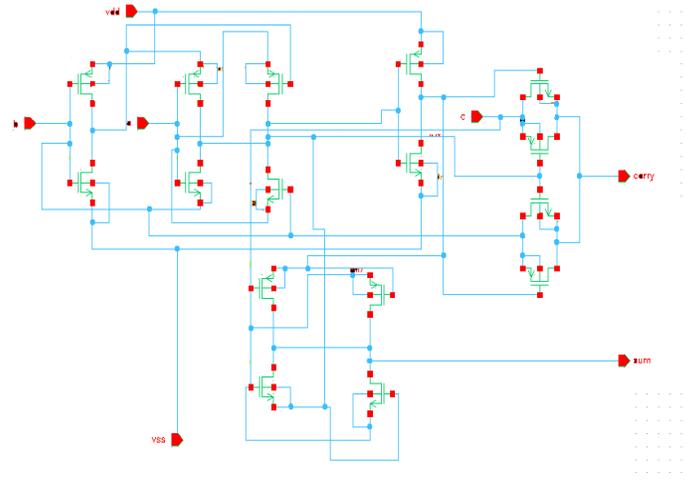


Figure.4. Hybrid adder schematic diagram

III. PROPOSED FULL ADDER

The proposed full adder circuit consists of fourteen transistors and is pictured by three blocks as shown in Fig. 5. Module one and Module two depicts the XNOR module that generates the total sum signal (SUM) and Module three generates the output carry signal (Cout). Every module is designed separately such entire adder circuit is optimized in terms of power, delay and chip size.

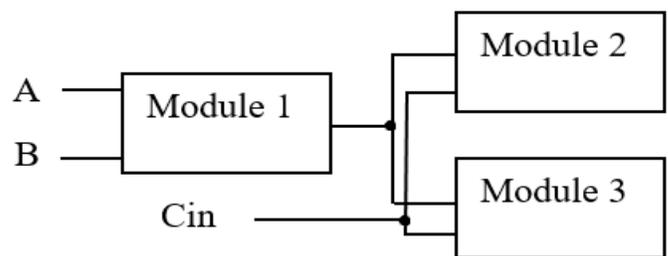


Figure.5. Block Diagram of Proposed Full Adder

Usually XNOR module is accountable for most of the ability power consumption of the complete module circuit [1]. Therefore, the proposed XNOR module is meant in such a way that it adapts solely 2 transistors in PTL. The output of XNOR module is fed into the XOR module which is designed using CCMOS inverter to generate SUM. We use TG and PTL. Since, PTL has the drawback of voltage degradation, TG has been used. In the proposed circuit, the output carry module is enforced by two TG. The deliberate use of robust TG guaranteed further reduction in propagation delay of the carry signal. Fig. 6 shows the proposed full adder (14T).

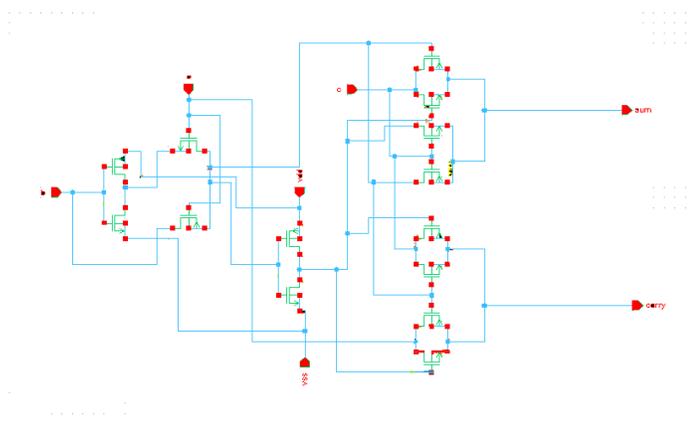


Figure.6. Proposed Full Adder 1 (14T)

IV. IMPLEMENTATION OF PROPOSED FULL ADDER

The proposed full adder is implemented on 2*2 braun multiplier. Multiplication is one of the most important operations in digital computer system because the performance of the processors is significantly influenced by the speed of their multipliers and adders. In order to achieve the high speed and low power demand in DSP applications braun multiplier are broadly used. The braun multiplier is also known as carry save array multiplier. The architecture of a braun multiplier consists of AND gates and full adders. In this paper AND gate is designed using a CCMOS logic style. CCMOS adder is also implemented on a braun multiplier for the comparative analysis in terms of power, delay and area.

V. RESULT AND DISCUSSION

A. Performance analysis of proposed full adder

The simulation of proposed full adder is carried out using 180nm technology and compared with the other existing adders. Comparative analysis between various types of full adder is shown in Table1. Comparison involves average power, delay and area. Fig. 7 and Fig. 8 depicts the average power and delay time of the proposed adder along with existing adders.

Table.1. Comparison of Different Design Styles with Proposed Adder

| Design technique | No. of transistors | Power (μW) | Delay (ps) |
|------------------|--------------------|-------------------------|------------|
| CCMOS | 28 | 198.8 | 96.34 |
| Hybrid | 16 | 116.7 | 1.978 |
| CPL | 32 | 852.5 | 4.1 |
| TFA | 16 | 109.2 | 1.062 |
| Proposed | 14 | 26.68 | 3.355 |

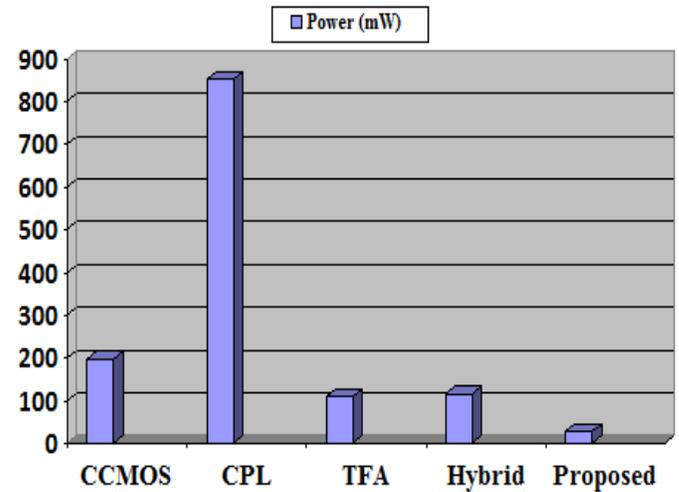


Figure.7. comparison analysis

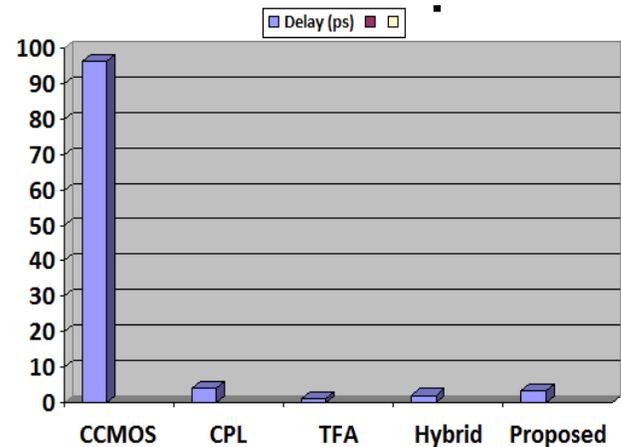


Figure.8. comparison analysis

B. Performance analysis of a braun multiplier using proposed adder

Table2 depicts the comparative analysis of braun multiplier using CCMOS and proposed adder.

Table.2. Comparison of Braun Multiplier

| Braun Multiplier designed using | Power (μW) | Delay (ps) |
|---------------------------------|-------------------------|------------|
| CCMOS | 45.17 | 107.8 |
| Proposed | 37.20 | 495.8 |

VI. CONCLUSION

In this paper, a hybrid 1-bit full adder has been proposed and the simulation is carried out using cadence virtuoso tool with 180nm technology. The proposed adder was compared with other existing design approaches such as CCMOS, CPL, TFA and hybrid design. The simulation results shows that the proposed full adder offered 86.57% improvement with regards to average power when compared to CCMOS full adder and the proposed adder was further enforced on a 2x2 multiplier which offered 18.04% improvement with respect to average power when compared to CCMOS based multiplier.

VII. REFERENCES

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