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Implementation of 8 Bit Dadda Multiplier for Fir Filters by Approximate Compressors

S.Senthil Sivamanikandan[1], J.Jesintha[2]
Assistant Professor[1], ME VLSI Student[2]
Department of Electronics and communication Engineering
Dr.Sivanthi Aditanar College of Engineering, India

Abstract:
The most area consuming arithmetic operations in high-performance circuit's Finite Impulse Response (FIR) multiplication is one. Approximate computing is an emerging trend in digital design that trades off the requirement of exact computation for improved speed and power performance. This paper proposes approximate compressors and an algorithm to exploit them for the design of efficient approximate multipliers. The proposed approximate compressors are designed and analyzed for dadda multiplier. The multiplier is implemented in fir filter design within the best area and power results. The simulation results are implemented for the filtering application by using Xilinx ISE design suite 14.5.

Keywords: Compressor, Approximate computing, Dadda multipliers

I.INTRODUCTION

Detecting Digital multipliers are among the most critical arithmetic functional units in many applications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The throughput of these applications depends on multipliers, and if the multipliers are too slow, the performance of entire circuits will be reduced. There is an apparently trade-off between accuracy and hardware complexity. Recently, compensation works have been increasing focused on reducing the truncation error on the Booth multiplier. Multipliers have been important since the introduction of the digital computers. Multiplication occurs frequently in Digital Signal Processing (DSP) systems, communication systems and other Application Specific Integrated Circuits (ASICs).

Because of the significance of multiplication in scientific and engineering computations, this area has received much attention in the past decades which has led to a number of implementation techniques for multiplication. Multipliers are key components of many high performance systems such as FIR filters, microprocessors, digital signal processors, etc. In Digital Signal Processing, FIR filters define less number of bits which are designed by using finite precision In IIR filter by using feedback problems will raise but in FIR filters limited bits are efficient in which there is no feedback. Using fractional arithmetic we can implement FIR filters. But in IIR filters, coefficients with magnitude of less than 1.0are always possible to implement a FIR filter.

Using FIR filters is that they require more co-efficient than an IIR filter in order to implement the same frequency response, therefore needing more memory and more hardware resources to carry out mathematical operations. For implementing the FIR filter we need multiplier, adder, delay & storage modules. Multiplier block has huge impact on complexity & performance of system as it requires huge no of Multiple Constant Multiplication / Accumulation.

II.8X8 DADDA MULTIPLIER

An 8×8 unsigned Dadda tree multiplier is considered to assess the impact of using the proposed compressors in approximate multipliers. Dadda multiplier is a hardware multiplier designed similar to Wallace multiplier. Unlike Wallace multipliers that perform reductions as much as possible on each layer, Dadda multipliers do as few reductions as possible. Due to this, Dadda multipliers have less expensive reduction phase, but the numbers may be a few bit longer, thus requiring slightly bigger adders. This implies that fewer columns are compressed in the initial stages of the column compression tree, and more columns in the later levels of the multiplier. The proposed multiplier uses in the first part AND gates to generate all partial products. In the second part, the approximate compressors proposed in the previous section are utilized in the CSA tree to reduce the partial products. The last part is an exact CPA to compute the final binary result. The reduction circuitry of an exact multiplier for n=8.

III.4:2 Compressor Design with Ao222 Compound Gate

The dadda multiplier is designed using the proposed approximate compressor with AO222 compound gate. a novel 4-2 compressor design that can be used in the partial product compression phase of a dadda multiplier. The proposed design uses a small modification of an existing 4-2 compressor design, low error rate approximate 4-2 compressor was designed by considering the characteristics of the AND gate that is used in partial product generation. The probability that a partial product bit equals 1 and 0 are 1/4 and 3/4, respectively. Thus, an input to a 4-2 compressor is three times more likely to be a 0 than a 1. Also, if there is no carry-in, a carry-out can only occur when all four input bits are 1. Denoting the two outputs of a 4-2 compressor as C and S and simply letting C,S equal 1,1 (instead of 00 with a carry-out of 1).

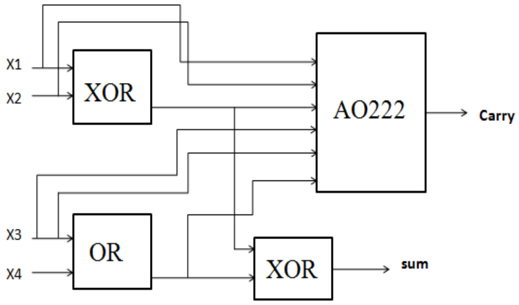


Figure.3.1 Approximate compressor using AO222 compound gate

The expression for sum and carry for the approximate compressor is

Carry=x1.x2+x1.x3+x1.x4+x2.x3+x2.x4+x3.x4

sum = (x1^x2)^(x3+x4)

Table.3.1. Truth table for approximate compressors with AO222 compound gate

X1	X2	X3	X4	C	S
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	1

In Table 3.1 approximate multiplier circuit is designed using the proposed 4-2 compressor design The red color denotes the error in the circuit. To rectify these errors a simple error recovery circuit is used for compensation. When all inputs (X*1*, X2, X*3*, and X4) are 1, Eqs (1) and (2) can be used for the carry C and sum S bits. This not only obviates the need for carry-in and carry-out bits, it also makes the resulting logic implementation simpler. The trade-off is a small loss in accuracy, as reflected in the truth table.

IV. NOVEL APPROXIMATE COMPRESSOR DESIGN

The dadda multiplier is designed using the 4:2 approximate compressor. A novel approximate compressor is proposed and dadda multiplier is designed to achieve high accuracy with less area. The proposed approximate compressors have *j* inputs *p*0, *p*1, . . . , *p j*−1 and compute *j* /2 outputs by using a novel approach aimed to minimize the error probability and the average error. For most of the combinations of *pi* they compute the same value as (2), while in some cases they give an error. This is different from standard compressors, where the weight of the carry output is two times the weight of the inputs.

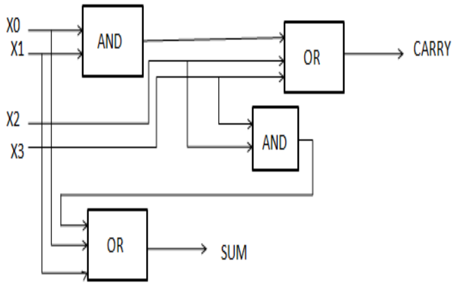


Figure.4.1 Novel Approximate compressor design

The expression for sum and carry for the novel approximate compressor is

Carry = X2+X3+(X0.X1)

Sum =X0+X1+(X2.X3)

Table. 4.1. Truth table for novel approximate compressor design

X1	X2	X3	X4	C	S
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	1	0
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Table 4.1 shows the behavior of the proposed approximate 4/2 compressor. For four *pi* combinations, we have an error of 1, while there is a unique partial products combination resulting in an error of 2.

V. IMPLEMENTATION OF FIR FILTER DESIGN

Digital filters have a magnificent role in various applications related to signal processing. It is the performance of the filters that made DSP popular. Filtering is usually done to obtain a desired output by manipulating the input data. Various types of filters are used to manipulate the data that helped in creating different applications to benefit the world. The major part in any filter design is the multiplication block as the performance of any filter depends on how the multiplication is performed. There are various multipliers of which Dadda multiplier is one, the significance of this is that it makes use of very few gates to perform multiplication.

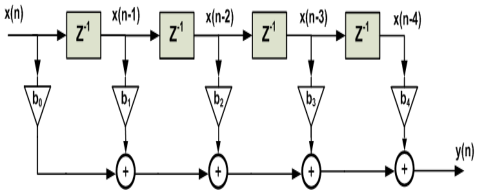


Figure.5.1 Design of FIR Filter

The FIR filter is generally used to compute weighted sum of an input signal by analyzing different types of multiply and accumulate operations. The structure of the filter is characterized by the difference equation which is represented with the basic elements like multipliers, time delays and adders.

The standard equation for FIR filter is as shown:

y[n]=b0x[n]+b1x[n-1]+b2x[n-2]+…..+bNx[n-N]

The input signal is multiplied by a series of constant coefficients. The input data is directed to either the sample register or the coefficient bank based on the input given to the control unit. The sample values are stored in the sample register whereas coefficient bank is used to store the coefficients. The coefficient bank is designed to store up to 256 coefficients. Accessing of each register is carried using rd_ptr or wr_ptr which are of 8 bit size. When the wr_en is high, coeff_wr is high and the coefficient value is stored in the registers. At the maximum, 256 number of coefficient values can be stored. If the sample_wr is high, data_in is sample and it is given to multiplier. If the rd_en is high then all the coefficient values are read from the coefficient bank one by one. The coefficient bank output and the sample output are given as inputs to the Dadda multiplier that multiplies and the output is given to Parallel Prefix adder. If fir_en is high then the multiplication and accumulation process continues, else the result stored in the fir register will be the output.

VI. EXPERIMENTAL RESULTS AND DISCUSSION

Both dadda multiplier using proposed compressors are implemeted in FIR filter design. The results of area , power, delay are compared and analyzed.

RTL schematic

The daada multiplier is implemented in fir filter design using approximate compressor with AO222 compound gate. The respective RTL diagram is shown in figure 6.1.

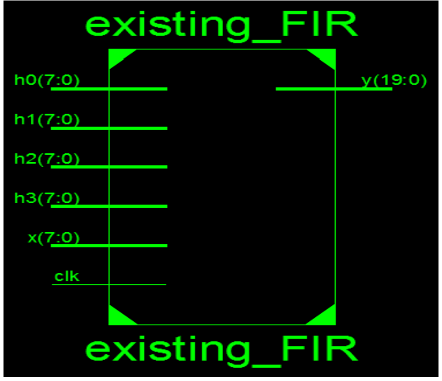
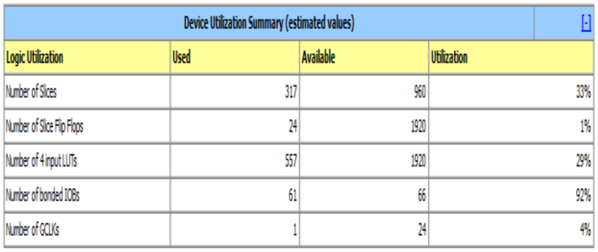


Figure.6.1. RTL schematic of FIR filter with A0222 compressor

Device utilization:

Figure 6.2 shows device utilization summary of fir filter design using approximate compressor with AO222 compound gate. Here the usage of slices is 347 and the numbers of 4 input LUTs are 557.The usage of bonded IOBs are 61. The number of bonded IOBs utilization percentage is 92%.



Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	317	960	33%
Number of Slice Flip Flops	24	1920	1%
Number of 4 input LUTs	557	1920	29%
Number of bonded IOBs	61	66	92%
Number of GCLKs	1	24	4%

Figure.6.2 Area analyzer of FIR filter with A0222 compressor

RTL schematic

The daada multiplier is implemented in fir filter design using novel approximate compressor The respective RTL diagram is shown in figure 6.3.

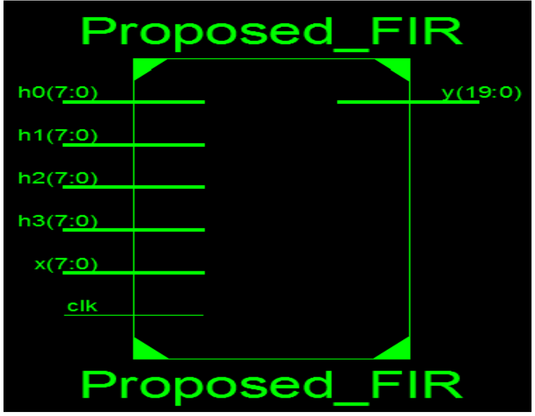
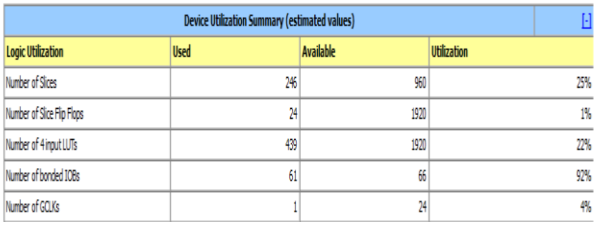


Figure.6.3. RTL schematic of FIR filter with novel approximate compressor

Device utilization

Figure 6.4 shows device utilization summary of fir filter design using novel approximate compressor. Here the usage of slices are 246 and the number of 4 input LUTs are 439.The usage of bonded IOBs are 61. The number of bonded IOBs utilization percentage is 92%.



Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	246	960	25%
Number of Slice Flip Flops	24	1920	1%
Number of 4 input LUTs	439	1920	22%
Number of bonded IOBs	61	66	92%
Number of GCLKs	1	24	4%

Figure .6.4 Area analyzer of FIR filter with novel approximate compressor

Comparison results

Table.6.1 Comparison between the FIR filter compressors design

Method used	Area	Power	Delay
FIR filter using approximate AO222 compressor	347 slices 557 LUTs 61 IOBs 24 flip flops	0.034W	27.372ns
FIR filter using novel approximate compressor	246 slices 439 LUTs 61 IOBs 24 flip flops	0.034W	26.923ns

VII. CONCLUSION

The approximate compressors are used to build dadda multipliers, using an algorithm that allocates the approximate compressors with the aim of optimize electrical performance while providing small error. The proposed approximate compressors are designed and analyzed for dadda multiplier and the multipliers are implemented in FIR filter design. Novel Approximate compressor FIR filter designs offer significant performance improvement compared to AO222 approximate compressor FIR filter design .The results of both fir filter design area, power, delay parameters are compared and analyzed. The simulation results are implemented for the filtering application by using Xilinx ISE design suite 14.5.

VIII. REFERENCES

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