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Non-Isolated Voltage Quadrupler DC-DC Converter with Low Switching Voltage Stress

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Abstract:
In this paper, a novel transformer-less adjustable voltage quadrupler DC–DC converter with high voltage transfer gain and reduced semiconductor voltage stress is proposed. The proposed topology utilizes input parallel and output series configuration for providing a much higher voltage gain without adopting an extreme large duty cycle. This proposed converter not only achieves high step-up voltage gain with reduced component count but also reduce the voltage stress of both active switches and diodes. This will allow choosing lower voltage rating MOSFETs and diodes to reduce both switching and conduction losses. In addition, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the two interleaved phases for voltage boosting mode without adding extra circuitry or complex control methods. The operation principle and steady state analysis as well as a comparison with other recent existing high step-up topologies are presented.

I. INTRODUCTION

In this chapter, a Non-isolated adjustable voltage quadrupler topology is proposed. It integrates two-phase interleaved boost converter to realize a high voltage gain and maintain the advantage of an automatic current sharing capability simultaneously.

Furthermore, the voltage stress of active switches and diodes in the proposed converter can be greatly reduced to enhance overall conversion efficiency. The remaining contents of this paper may be outlined as follows. First, the circuit topology and operation principle are given. Then, the corresponding steady state analysis is made to provide some basic converter characteristics.

II. LITERATURE REVIEW

For high efficiency, the SMPS switch must turn on and off quickly and have very less losses. The main DC-DC converters were developed in the early 1960s when semiconductor switches were available. Switched systems such as SMPS are a challenge to design since its model depends on whether a switch is opened or closed. R. D. Middle brook from Caltech in 1977 published the models for DC-DC converters in market today.

He averaged the circuit configurations for each switch state in a technique called state space average modeling. This simplification resulted in reduction of two systems into one. This model led to insightful design equations which helped growth of SMPS [1]. Many topologies have been presented to provide a high step-up voltage gain without an extremely high duty ratio. A DC–DC fly back converter is a very simple isolated structure with a high step-up voltage gain, but the active switch of this converter will suffer a high voltage stress due to the leakage inductance of the transformer. For recycling the energy of the leakage inductance and minimizing the voltage stress of the active switch, some energy regeneration techniques have been proposed to clamp the voltage stress on the active switch and to recycle the leakage inductance energy [2], [3]. Some existing isolated voltage type converters, such as the phase shifted full bridge converters, can achieve a high step-up gain by increasing the turns ratio of the transformer. Unfortunately, the higher input current ripple will reduce the maximum output power and shorten the usage life of input electrolytic capacitor.

To reduce the effects, more input electrolytic capacitors are required to suppress the large input current ripple. Furthermore, the output diode voltage stress is much higher than the output voltage, which will degrade the circuit efficiency in the high output voltage applications. Other isolated current type converters, such as the active clamp dual boost converters and the active clamp full bridge boost converters can realize high efficiency and high step-up conversion [4],[5].

However, the start-up operation of these converters must be considered separately. Moreover, the cost is increased because many extra power components and isolated sensors or feedback controllers are required. In order to reduce system cost and to improve system efficiency, a non-isolated DC-DC converter is in fact, a more suitable solution.

III. BOOST CONVERTER

The DC-DC boost converters are used to convert the unregulated DC input to a controlled DC output at a desired voltage level. They generally perform the conversion by applying a DC voltage across an inductor or transformer for a period of time which causes current to flow through it and store energy magnetically, then switching this voltage off and causing the stored energy to be transferred to the voltage

output in a controlled manner. The output voltage is regulated by adjusting the ratio of on time to off time.

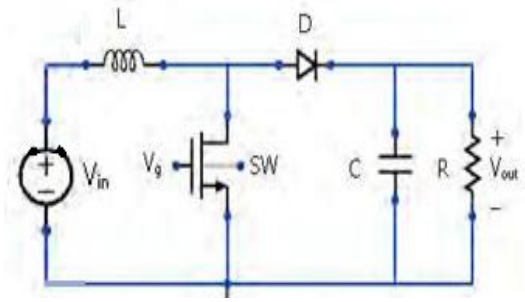


Figure. 4.1 Schematic of Boost converter.

$$\frac{vo}{vi} = \frac{1}{1-D}$$

The above equation shows that the output voltage is always higher than the input voltage (as the duty cycle goes from 0 to 1), and that it increases with D, the or ethically to infinity as D approaches 1. This is why this converter is sometimes referred to as a step-up converter.

Rearranging the equation reveals the duty cycle to be:

$$D = 1 - \frac{V_o}{V_i} \qquad D$$

IV.VOLTAGE QUADRUPLER

5.1 Operating Principle

For convenient reference, the two-phase interleaved boost converter with parallel input and series output connection is first shown in Fig. 5.1(a). The proposed converter topology is basically derived from a two-phase interleaved boost converter and is shown in Fig. 5.1(b). Comparing Fig. 5.1(a) with Fig. 5.1(b), one can see that two more capacitors and two more diodes are added so that during the energy transfer period partial inductor stored energy is stored in one capacitor and partial inductor stored energy together with the other capacitor stored energy is transferred to the output to achieve much higher voltage gain. However, the proposed voltage gain is twice that of the interleaved two-phase boost converter. Also, the voltage stresses of both active switches and diodes are much lower than the latter. Furthermore, the proposed converter possesses automatic uniform current sharing capability without adding extra circuitry or complex control methods. The detailed operating principle can be illustrated as follows.

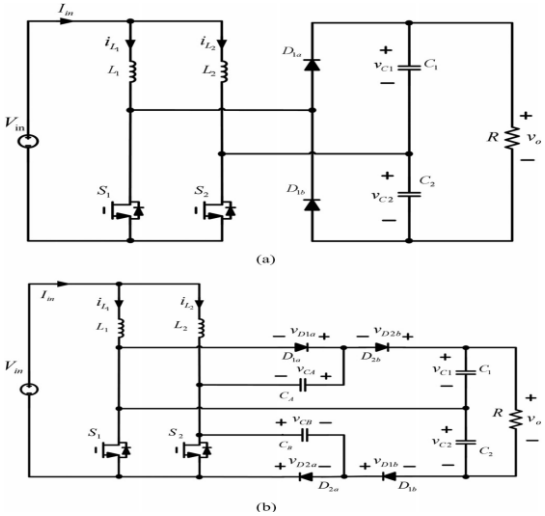


Figure.1. Configurations of (a) two-phase interleaved boost converter, (b) the proposed converter.

As the main objective is to obtain high voltage gain and such characteristic can only be achieved when the duty cycle is greater than 0.5 and in continuous conduction mode (CCM); hence, the steady-state analysis is made only for this case. However, with duty cycle lower than 0.5 or in DCM, as there is no enough energy transfer from the inductors to the blocking capacitors, output capacitors, and load side, and consequently it is not possible to get the high voltage gain. In addition, only with duty cycle larger than 0.5, due to the charge balance of the blocking capacitor, the converter can feature the automatic current sharing characteristic that can obviate any extra current-sharing control circuit. On the other hand, when duty cycle is smaller than 0.5, the converter does not possess the automatic current sharing capability any more, and the current-sharing control between each phases should be taken into account in this condition.

In order to simplify the circuit analysis of the proposed converter, the following assumptions are made.

1) All components are ideal components.

2) The capacitors are sufficiently large, such that the voltages across them can be considered as constant approximately.

3) The system is under steady state and is operating in CCM and with duty ratio being greater than 0.5 for high step-up voltage purpose.

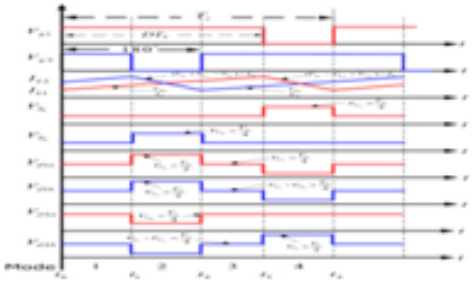


Figure.2. Waveforms of the proposed converter at Continuous Conduction Mode.

Basically, the operating principle of the proposed converter can be classified into four operation modes. The interleaved gating signals with a 180° phase shift as well as some key operating waveforms are shown in Fig. 5.2. **Mode 1 ($t_0 \le t < t_1$)**: For mode 1, switches S_1 and S_2 are turned ON, D_{1a}, D_{1b},D_{2a},D_{2b} are all OFF. The corresponding equivalent circuit is shown in Fig. 5.3(a). From Fig. 5.3(a), it is seen that both i_{L1} and i_{L2} are increasing to store energy in L_1 and L_2, respectively. The voltages across diodes D_{1a} and D_{2a} are clamped to capacitor voltage V_{CA} and V_{CB}, respectively, and the voltages across the diodes D_{1b} and D_{2b} are clamped to V_{C2}minus V_{CB} and V_{C1} minus V_{CA}, respectively. Also, the load power is supplied from capacitors C_1 and C_2.

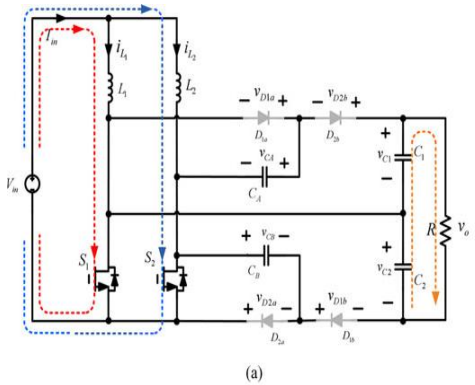
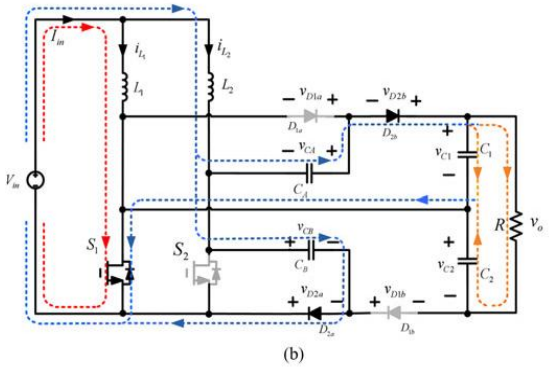


Figure.3. (a) Equivalent circuit of the proposed converter in Mode 1 and Mode 3.

Mode 2 ($t_1 \le t < t_2$): For this operation mode, switch S_1remains conducting and S_2 is turned OFF. Diodes D_{2a} and D_{2b} become conducting. The corresponding equivalent circuit is shown in Fig. 5.3(b). It is seen from Fig. 5.3(b) that part of stored energy in inductor L_2 as well as the stored energy of C_A is now released to output capacitor C_1 and load. Mean while, part of stored energy in inductor L_2 is stored in C_B. In this mode, capacitor voltage V_{C1} is equal to V_{CB} plus V_{CA}. Thus,i_{L1} still increases continuously and i_{L2} decreases linearly. The corresponding state equations are given as follows:

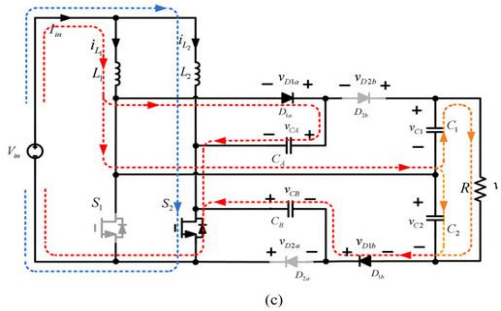


(b)

Figure.4. (b) Equivalent circuit of the proposed converter in Mode 2.

Mode 3 ($t_2 \le t < t_3$): For this operation mode, as can be observed from Fig. 5.3(a), both S_1 and S_2 are turned ON. The corresponding equivalent circuit turns out to be the same as Fig. 5.3(a).

Mode 4($t_3 \le t < t_4$): For this operation mode, switch S_2remains conducting and S_1 is turned OFF. Diodes D_{1a} andD_{1b} become conducting. The corresponding equivalent circuit is shown in Fig. 5.3(c). It is seen from Fig. 5.3(c) that the part of stored energy in inductor L_1 as well as the stored energy of C_B is now released to output capacitor C_2 and load. Meanwhile, part of stored energy in inductor L_1 is stored in C_A. In this mode, the output capacitor voltage V_{C2} is equal to V_{CB} plus V_{CA}. Thus,i_{L2} still increases continuously and i_{L1} decreases linearly. The corresponding state equations are given as follows:



(c)

Figure.5. (c)Equivalent circuit of the proposed converter in Mode 4.

From the above illustration of the proposed converter, one can see that the operations of two phase are both symmetric and rather easy to implement. Also, from key operating waveforms of the proposed converter is shown in Fig.5.2. One can see the low voltage stress of two active switches and four diodes as well as the uniform current sharing.

5.2 Steady State Analysis

In order to simplify the circuit performance analysis of the proposed converter in CCM, the same assumptions made in the previous section will be adopted.

5.2.1. Voltage Gain

Referring to Fig. 5.3(a) and 5.3(c), from the volt second relationship of inductor $L_1$and L_2, one can obtain the following relations:

$$V_{\text{in}}D + (V_{\text{in}} - V_{CA})(1-D) = 0 \quad \text{-------(5.1)}$$

$$V_{\text{in}}D + (V_{\text{in}} - V_{CB})(1-D) = 0. \quad \text{--------(5.2)}$$

Also from the equivalent circuits in Fig. 5.3(b) and 5.3(c), voltage V_{C1} and V_{C2} can be derived as follows by substituting the V_{CA} and V_{CB} solutions of (5.1) and (5.2):

$$V_{C1} = V_{CA} + V_{CB} = \frac{2}{1-D}V_{\text{in}} \quad \text{--------(5.3)}$$

$$V_{C2} = V_{CA} + V_{CB} = \frac{2}{1-D}V_{\text{in}}. \quad \text{------(5.4)}$$

It follows from (5.3) and (5.4) that the output voltage cans be obtained as follows:

$$V_o = V_{C1} + V_{C2} = \frac{4}{1-D}V_{\text{in}}. \quad \text{------(5.5)}$$

Thus, the voltage conversion ratio M of the proposed converter can be obtained as follows:

$$M = \frac{V_o}{V_{\text{in}}} = \frac{4}{1-D}. \quad \text{-----(5.6)}$$

5.2.2. Voltage Stresses on Semiconductor Components

To simplify the voltage stress analyses of the components of the proposed converter, the voltage ripples on the capacitors are ignored. From Fig. 5.3(b) and Fig.5.3(c), one can see that the voltage stresses on active power switches S_1 and S_2 can be obtained directly as shown in the following equation:

$$V_{S1,\max} = V_{S2,\max} = \frac{1}{1-D}V_{\text{in}}. \quad \text{--------(5.7)}$$

Substituting (5.5) into (5.6), the voltage stresses on the active power switches can be expressed as

$$V_{S1,\max} = V_{S2,\max} = \frac{V_O}{4}. \quad \text{-------(5.8)}$$

From (5.8), one can see that the voltage stress of active switches of the proposed converter is equal to one fourth of the output voltage. Hence, the proposed converter enables to adopt lower voltage rating devices to further reduce both switching and conduction losses. As can be observed from the equivalent circuits in Fig. 5(a) and Fig. 5(c), the open circuit voltage stress of diodes D_{1a}, D_{2a}, D_{1b}, and D_{2b} can be obtained directly as shown in(5.9).

$$V_{D1a,\max} = V_{D1b,\max} = V_{D2b,\max} = \frac{V_O}{2}, V_{D2a,\max} = \frac{V_O}{4}. \quad \text{---(5.9)}$$

In fact, it can seen from (5.9) that the maximum resulting voltage stress of diodes is equal to Vo /2. Hence, the proposed converter enables one to adopt lower voltage rating diodes to further reduce conduction losses.

5.2.3. Characteristic of Uniform Input Inductor Current Sharing

By using the state space averaging technique, one cans repeat the previous process to get the averaged state equations quite

straight forward as follows:

$$L_1\frac{di_{L1}}{dt} = V_{in} - (1-D)V_{CA} \quad \text{------(5.10)}$$

$$L_2\frac{di_{L2}}{dt} = V_{in} - (1-D)V_{CB} \quad \text{--------(5.11)}$$

$$C_A\frac{dv_{CA}}{dt} = \frac{(1-D)C_A\left(C_{eq1}I_{L1}(C_2+C_B) - C_{eq2}I_{L2}C_1\right)}{C_{eq1}C_{eq2}} - \frac{(1-D)C_AC_B\left(C_{eq1}+C_{eq2}\right)(V_{C1}+V_{C2})}{C_{eq1}C_{eq2}R} \quad \text{-(5.12)}$$

$$C_B\frac{dv_{CB}}{dt} = \frac{(1-D)C_B\left(C_{eq2}I_{L2}(C_1+C_A) - C_{eq1}I_{L1}C_2\right)}{C_{eq1}C_{eq2}} - \frac{(1-D)C_AC_B\left(C_{eq1}+C_{eq2}\right)(V_{C1}+V_{C2})}{C_{eq1}C_{eq2}R} \quad (5.13)$$

$$C_1\frac{dv_{C1}}{dt} = \frac{(1-D)C_1\left(C_AI_{L2}R - (C_A+C_B)(V_{C1}+V_{C2})\right)}{C_{eq1}R} - \frac{D(V_{C1}+V_{C2})}{R} \quad \text{----(5.14)}$$

$$C_2\frac{dv_{C2}}{dt} = \frac{(1-D)C_2\left(C_BI_{L1}R - (C_A+C_B)(V_{C1}+V_{C2})\right)}{RC_{eq2}} - \frac{D(V_{C1}+V_{C2})}{R} \quad \text{----(5.15)}$$

where I_{L1}, I_{L2}, V_{CA}, V_{CB}, V_{C1} and V_{C2} denote the average state variables, I_{L1}, I_{L2}, V_{CA}, V_{CB}, $V_{C1}$and V_{C2} represent the corresponding dc values. $C_{eq1} = C_1C_A+C_1C_B+C_AC_B$, $C_{eq2} = C_2C_A+C_2C_B+C_AC_B$, and $I_o = (V_{C1}+V_{C2})/R$. By selecting $C_1 = C_2 = C_x$, $C_A = C_B = C_y$, one can get the corresponding dc solutions as follows:

$$I_{L1} = I_{L2} = \left(\frac{2}{1-D} + \frac{DC_y}{(1-D)C_x}\right)I_o, \quad \text{----(5.16)}$$

5.3. Performance Comparison

For demonstrating the performance of the proposed converter and its performance is compared with some recent high step-up converters introduced shown in Table 5.3

Table .1. Comparison of the steady state characteristics.

	Conventional Boost Converter	Voltage doubler	High step-up ratio dc–dc converter	Ultra High Step up Converter	Voltage Quadrupler
Voltage gain	$\frac{1}{1-D}$	$\frac{2}{1-D}$	$\frac{3-D}{1-D}$	$\frac{3+D}{1-D}$	$\frac{4}{1-D}$
Voltage Stress of Switches	1	$\frac{1}{2}$	$\frac{1}{3-D}$	$\frac{2}{3+D}$	$\frac{1}{4}$
Voltage Stress of Diodes	1	1	$\frac{2}{3-D}$	$\frac{2}{3+D}$	$\frac{1}{2}$

Table 5.3 summarizes the voltage gain and normalized voltage stress of active as well as passive switches for reference. As an illustration, Fig. 5.4 shows the corresponding characteristic curve of the proposed converter.

For comparison, the voltage stress is normalized by the output voltage V_o , the voltage gains, the normalized switch stresses and the normalized output diode stresses of the conventional voltage doubler, high step-up ratio converter, and the ultrahigh step-up converter are also shown in the same figure to provide better view.

It is seen from Table 5.3that the proposed converter can achieve higher voltage gain than that of the other three boost converters.

Therefore, the proposed converter is rather suitable for use in applications requiring high step-up voltage gain. From Table 5.3, one can see that the proposed converter cans achieve the lowest voltage stress for the active switches.

Also, it is seen that it can achieve the lowest voltage stress for the diodes. As a result, one can expect that with proper design, it can adopt switch components with lower voltage ratings to achieve higher efficiency.

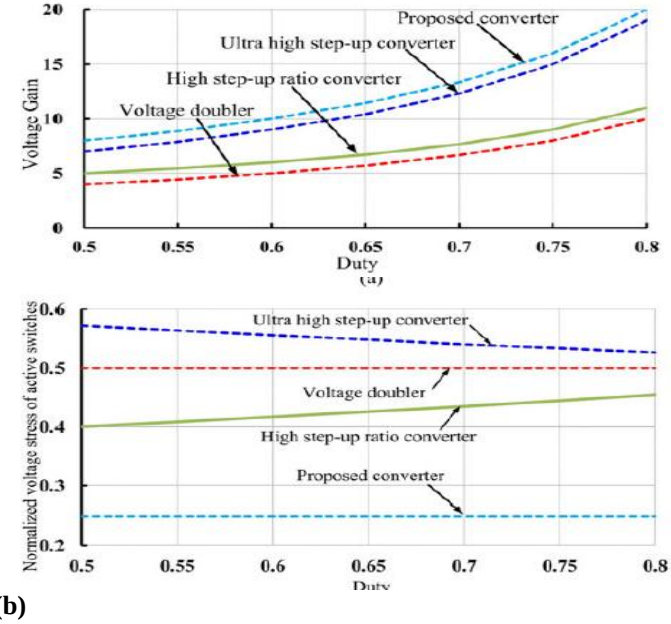


Figure.6. Comparison of the steady-state characteristics for four different converters (a) voltage gain (b) normalized voltage stress of active switches.

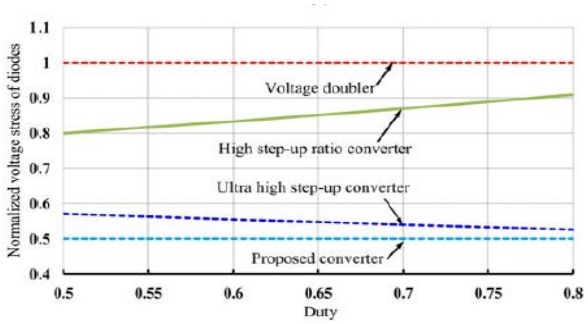


Figure.7. Comparison of the steady-state characteristics for four different Converters, (c) normalized voltage stress of diodes.

6.1 Simulation Model of Open Loop Control

The values of input voltages, switching frequency, inductances, capacitances and Load resistance are shown below. Its corresponding model is shown in Fig. 5.1 V_s = 25 V, V_o= 394 V,f=40 kHz,L_1=253µH,L_2= 253µH, C_a=10µ F,C_b=10µF,C_1 =250µF, C_2=250µF,R=400Ω,$V_{o(RMS)}$ = 394 V.

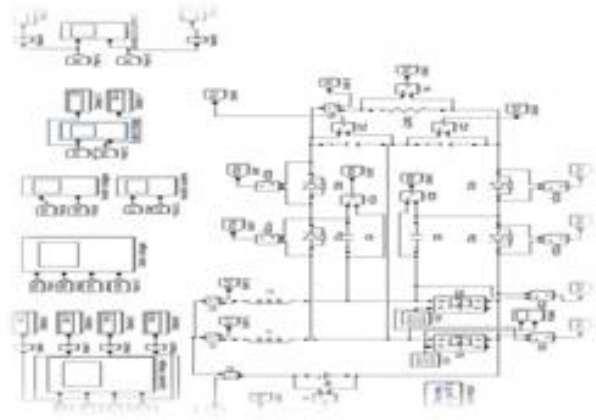


Figure.8. open loop voltage quadrupler with R load.

When compared with boost converter, VRF and CRF are low in quadrupler.

6.1.1 Simulation Results

Output voltage vs time is plotted in Fig. 6.2

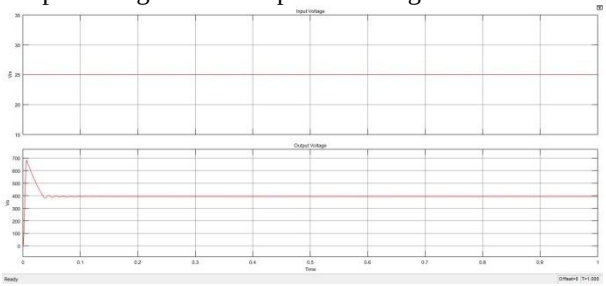


Figure.9. Waveforms of input and output Voltages.

From output voltage waveform shown in Fig. 6.2 voltage ripple factor is calculated and its value is 0.00006% which is less than VRF of boost converter. Also from Fig. 6.2 it is observed that output voltage is 394 V.

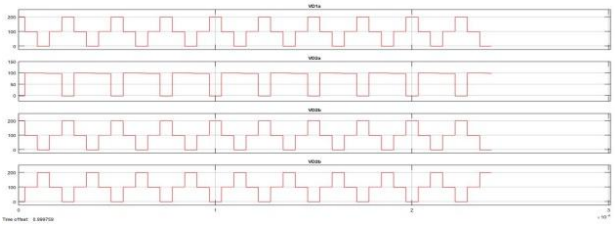


Figure.10. Waveforms of diode Voltages.

From Fig. 6.3, the maximum reverse voltage across Diodes D_{1a}, D_{1b}, D_{2b} is 196.5V = V_o/2 i.e., voltage stress of above diodes is0.5. But the maximum reverse voltage across Diodes D_{2a} is98.25V = V_o/4i.e., voltage stress of diode D_{2a}is0.25.

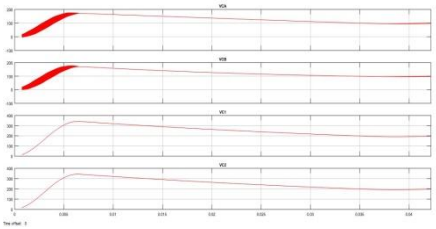


Figure.11. Waveforms of capacitor voltages Vca, Vcb, Vc1, Vc2.

From Fig. 6.4voltage across capacitors. Vca&Vcb is 98.25 V which is 1/4th of output voltage and voltage across capacitors Vc1& Vc2 is 196.5 V which is equal to Vo/2.

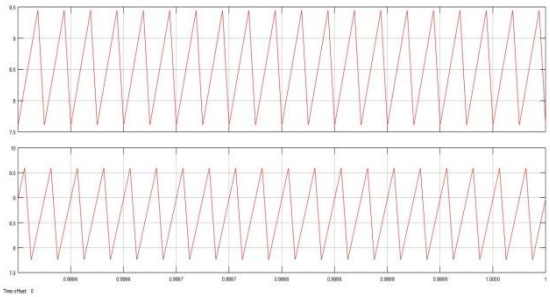


Figure.12. Waveforms of Stead State Inductor currents I_{L1}, I_{L2} Simulation results.

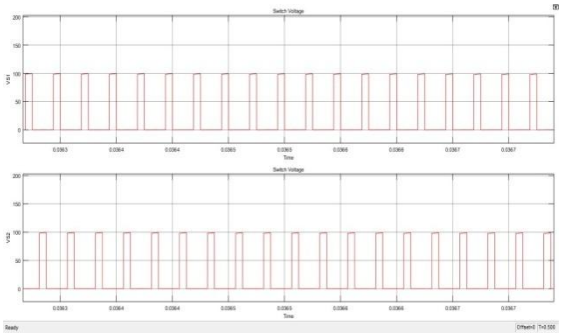


Figure.13. Waveforms of switch voltages V_{s1}, V_{s2}.

From Fig. 6.5 maximum ripple current in inductor is 4 A. From Fig.6.6, the maximum reverse voltage across switches is 100V ~ V_o/4i.e., voltage stress of switches is 0.25.

6.2 Simulation Model of Open Loop with RL Load

The values of input voltage, inductance, capacitances, load parameters are shown below

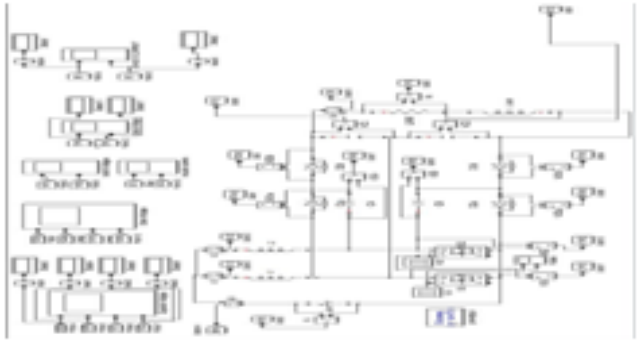


Figure.14. Voltage quadrupler open loop with RL load.

Model of an Open Loop Control of Non-isolated Voltage

Quadrupler DC-DC converter with RL load is shown in Fig. 6.8 V_s = 25 V, V_o= 394 V,f=40 kHz,L_1=253µH,L_2= 253µH,C_a=10µF,C_b=10µF,C_1=250µF, C_2=250µF,R=400Ω, L= 100 mH,$V_{o(RMS)}$ = 394 V.

6.2.1 Simulation Results

Output voltage vs time is plotted in Fig. 6.9

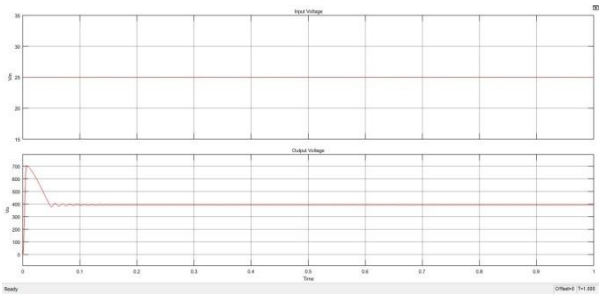


Figure.15. Waveforms of input and output Voltages.

From the output voltage waveform shown in Fig. 6.9 VRF is calculated and its value is 0.00004%. And output voltage is 394 V.

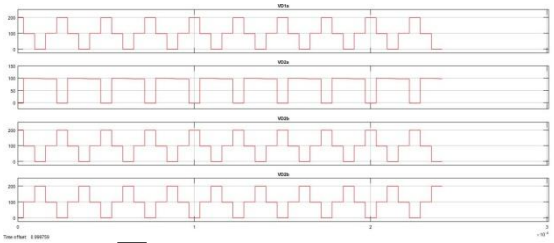


Figure.16. $\overline{10}$ Diode voltage waveforms.

From Fig. 6.10, the maximum reverse voltage across Diodes D_{1a},D_{1b},D_2 is 196.5V = Vo/2i.e., voltage stress of above diodes is0.5. But the maximum reverse voltage across Diodes D_{2a} is 98.25V = Vo/2 i.e., voltage stress of diode D_{2a} is 0.25

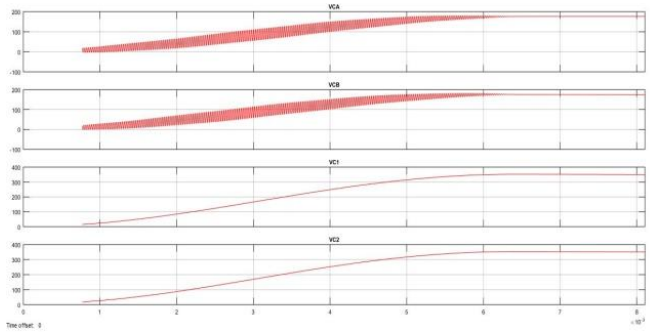


Figure.17. 11Capacitor voltage waveforms.

From Fig. 6.11 voltage across capacitors Vca&Vcb is 98.25 V which is 1/4th of output voltage and voltage across capacitors Vc1& Vc2 is 196.5 V which is equal to Vo/2.

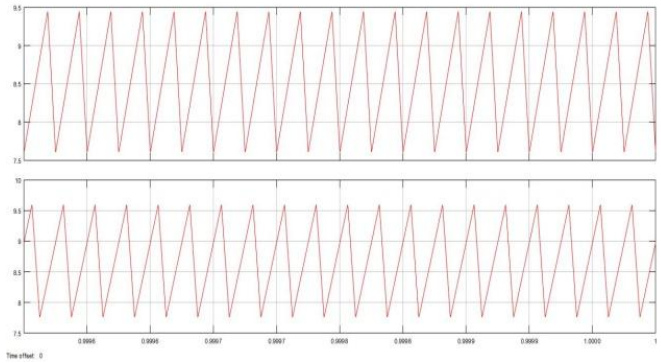


Figure.18.12Waveforms of Steady StateInductor current I_{L1}, I_{L2}.

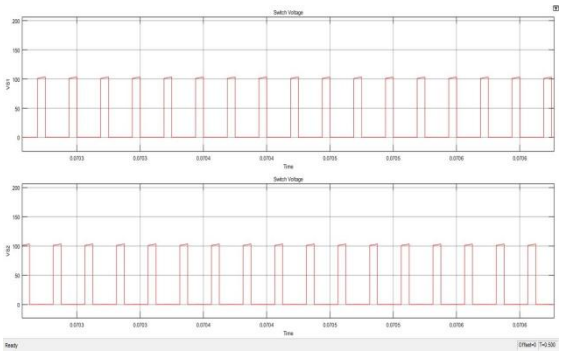


Figure.19. 13 Switching voltage waveforms.

From Fig. 6.12, the current ripples of inductor currents are nearly 4A. The interleaved structure can effectively increase the switching frequency and reduce the input and output ripples as well as the size of the energy storage inductors. Since input current I_{in} is equal to IL1 plus IL2, it is obvious that with the two-phase interleaving control, both input current ripples and switch conduction losses can be reduced. From Fig.6.13

V.CONCLUSION

In this chapter simulation of voltage quadrupler along with its results are discussed. From these results it can be concluded that the output of voltage quadrupler is high with less switching stress along with low reverse voltage across the diodes.

VI. REFERENCES

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