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Design of Low Power and High Performance Carry Save Adder Using Dynamic Logic

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Abstract:
Adders are the basic building block of any processor or data path application. For the design of high performance processing units high speed adders with low power consumption is required. To design efficient integrated circuits in terms of area, power and speed has become a challenging task in modern VLSI design field. In this paper the power and delay modified carry save adder is compared with the conventional Carry Save Adder (CSA) and the Domino logic based CSA. And also the proposed logic CSA is compared with the Ripple Carry Adder and Carry Bypass Adder. The proposed design is validated by implementation of 3 bit Carry Save Adder in a standard 90nm CMOS technology. This circuits is implemented using DSCH Tool, Microwind Tool.

Keywords: Carry Save Adder, Ripple Carry Adder, Carry Bypass Adder, Dynamic Logic, Domino Logic, Delay and power consumption.

I. INTRODUCTION:

High performance, energy- efficient logic style has always been a popular research topic in the field of very large scale integrated (VLSI) circuits because of the continuous demand of ever increasing circuit operating frequency. Recent technology scaling and use of various logic families provides techniques to achieve power consumption at the cost of performance. Power, speed and robustness are so critical to leading edge designs that they need to be taken care of each level of design. The choice of logic styles is a very important constraint at the circuit level. Logic styles differ in terms of energy, delay, area and robustness. Because every design requires compromises and trade-offs, designers need to pick and choose circuits from different points on an energy delay robustness envelope to meet each circuit need. Among other things, meeting the needs of future computing will require logic style that satisfies high-performance, low-power, high robustness in the form of noise and variability, ease of implementation and verification. In addition to that, we want to use logic styles that are compatible for all types of logic implementation for further improvement in robustness. The objective of this research work is to modify and improve domino logic that can provide further improvement in power consumption, performance, speed and area overhead.

I. The main objective is to reduce the delay, area and power consumption.

II. The performance of the system is high, hence the speed increases.

II. EXISTING ADDERS

A. Conventional Carry Save Adder(CSA)

Carry save adder is abbreviated as the CSA showed in in fig1. As we all know that adders are used for arithmetic functions in data processors. A carry-save adder is a type of digital adder, used in computer microarchitecture to compute the sum of three or more *n*-bit numbers in binary. It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another which is a sequence of carry bits.

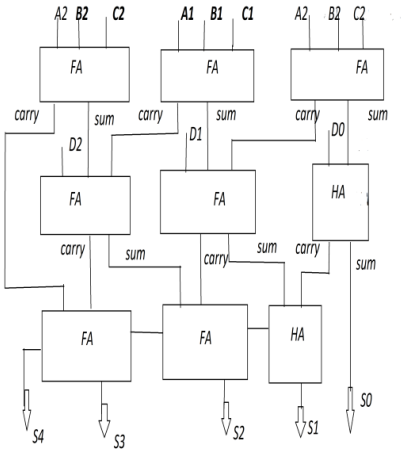

Figure.1. Conventional CSA

Carry save adder is consists of three or more n-bit binary numbers. Carry save adder is similar as full adder. Here we are computing sum of 3-bit binary numbers, so we take 3 full adders at first stage. Carry save unit consists of 6 full adders, each of which computes single sum and carry bit based only on the corresponding bits of the two input numbers. Let X and Y are two 3-bit numbers and produces partial sum and carry as S and C as shown in the Table 1.

Si = Xi xor Yi
Ci = Xi and Yi

Table 1. Carry save Adder Computation

X: 1 0 0 1 1
Y: 1 1 0 0 1
Z:+0 1 0 1 1

S: 0 0 0 0 1
C:+1 1 0 1 1

Sum: 1 1 0 1 1 1

The addition is then computed as:

1. Shifting the carry C left by one place.

2. Placing a 0 in front (MSB) of the partial sum sequence S.
3. Finally, a carry propagate adder is used to add these Two sequences together and computing the resulting sum.

B. DOMINO Full Adder:

Full adder cell realization uses 27 transistors as shown in Figure.2.It has lower delay as compared to static adder circuit having 28 transistor counts. It is based on the 3 transistor implementations of XOR and XNOR functions presented in, pass transistors and transmission gates. This circuit has several advantages, First, it reduces the number of transistor count which decreases the cell area as well as delay. Second, It balances the delays of generating XOR and XNOR, which lead to fewer glitches at the output. The output of full adder cell SUM and COUT can be produced using intermediate signal K = (B⊕C)' or K' = B⊕C.

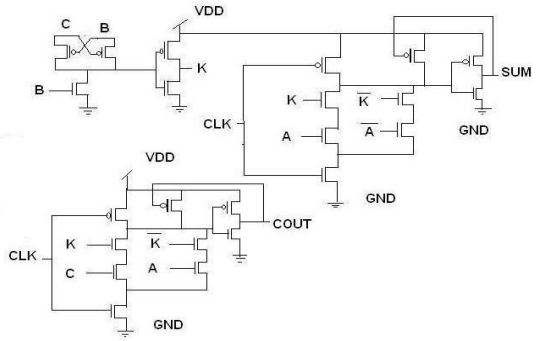

Figure.2. Full adder with Domino logic

C. RIPPLE CARRY ADDER:

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurance of the corresponding output. Consider a NOT gate, When the input is "0" the output will be "1" and vice versa. The time taken for the NOT gate's output to become "0" after the application of logic "1" to the NOT gate's input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurance of the carry out (Cout) signal. Figure 3 shows Ripple Carry Adder .

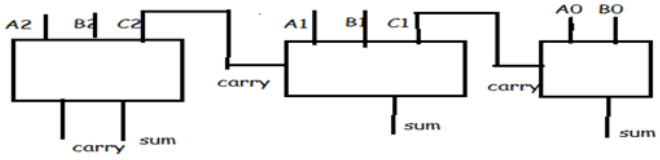

Figure.3.Ripple Carry Adder block diagram

D. CARRY BYPASS ADDER:

Carry Bypass is an adder implementation that improves on the delay of a Ripple Carry Adder with little effort compared to others. It has low power dissipation and high performance operation. If a full adder n generate a carry it will be the input for the independent carryin(Cin).Carry Bypass is more efficient than carry select adder, showed in figure 4.

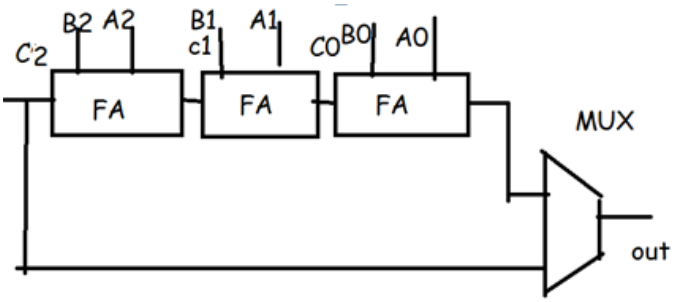

Figure.4. Carry Bypass Adder

III.PROPOSED LOGIC:

Dynamic logic:

Dynamic CMOS circuits had better performance and require less silicon area than conventional static CMOS circuits.The dynamic stage of all domino CMOS is compared of N logic and eliminates the internal race conditions by using a buffer at the output of every stage that produces only monitoring signal. Dynamic logic is distinguished from so-called *static logic* in that dynamics logic uses a clock signal in its implementation of combinational logic circuits. The usual use of a clock signal is to synchronize transitions in sequential logic circuits. For most implementations of combinational logic, a clock signal is not even needed.Figure 5 shows the domino logic.

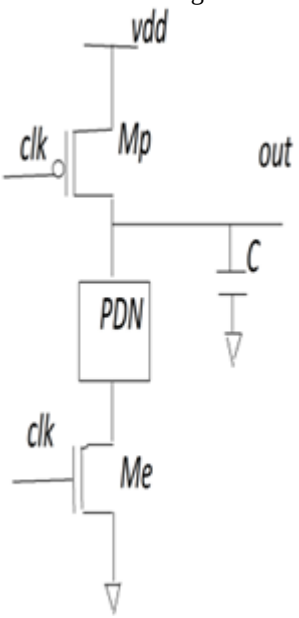

Figure.5. Dynamic logic

In integratedcircuit design, dynamiclogic (orsometimes clocke d logic) is a design methodology in combinatory logic circuits, particularly those implemented in MOS technology. It is distinguished from the so-called static logic by exploiting temporary storage of information in stray and gate capacitances. It was popular in the 1970s and has seen a recent resurgence in the design of high speed digital electronics, particularly computerCPUs. Dynamic logic circuits are usually faster than static counterparts, and require less surface area, but are more difficult to design. Dynamic logic has a higher toggle ratethan static logic but the capacitative loadsbeing toggled are smallerso the overall power consumption of dynamic logic may be higher or lower depending on various tradeoffs.

Full Adder using dynamic:

Full adder is the basic block for the addition process. In all the types of adders full adder places a main role. In order to make it with low power dissipation and delay means it can be implemented in several types of adders in order to improve the

performance of adders, multipliers and processors. Truth table showed in table 2.

Table .2. Full adder truth table

Cin	A	B	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

BLOCK DIAGRAM:

Full adder with dynamic logic is shown in fig 6. Power dissipation can be minimized by keeping load capacitance low. Clock signal is used to synchronize transition in sequential logic circuits.

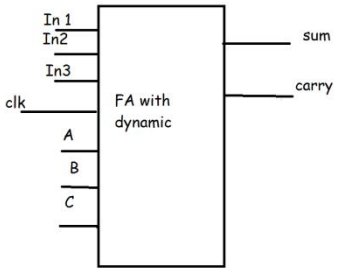

Figure.6. Full adder with dynamic

BLOCK DIAGRAM OF CARRY SAVE ADDER:

Carry Save Adder block diagram is shown in fig 7. Dynamic logic implemented full adder has used in the design of carry save adder in order to reduce power dissipation as well as delay. Carry save adder is a combination of half adder and full adder.

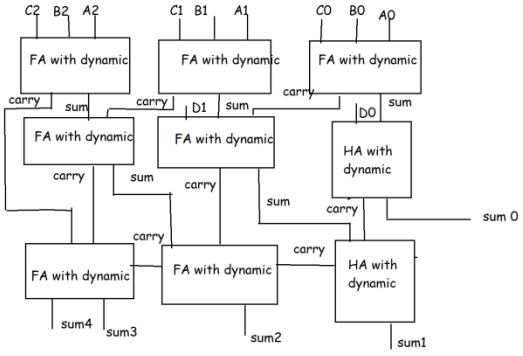

Figure.7. Carry save adder with dynamic block

Output Graph:

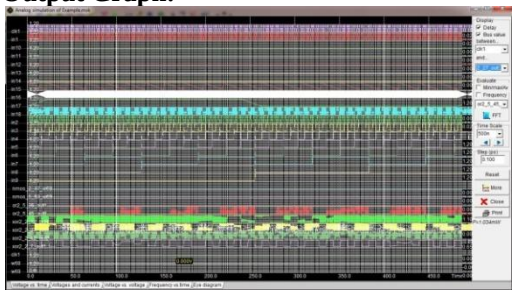

Figure.8.output graph conventional CSA

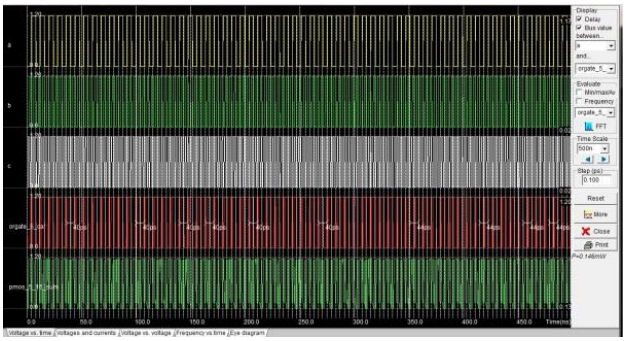

Figure.9. output graph of domino csa

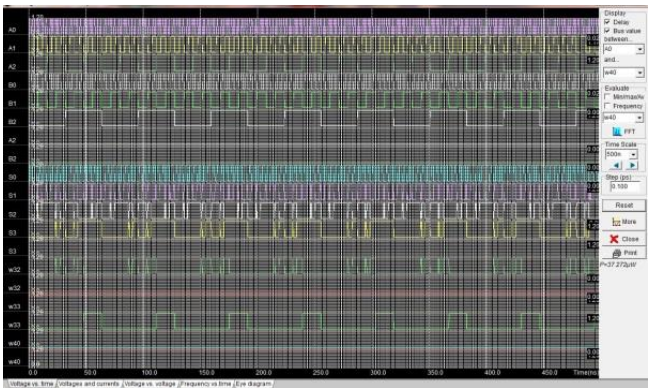

Figure.10.output of dynamic csa

COMPARISON TABLE 3:

3a. 3 – Bit RCA:

Parameter	Conventional	Domino	Dynamic
Power(uw)	40.661	70.958	36.280
Delay(ps)	80	75	60

3b. 3 – Bit CBA:

Parameter	Conventional	Domino	Dynamic
Power(mw)	0.195	0.300	0.193
Delay(ps)	73	39	34

3c. –3 Bit CSA:

Parameter	Conventional	Domino	Dynamic
Power(uw)	43.843	56.783	32.75
Delay(ps)	46	35	7

IV. CONCLUSION:

A new high performance proposed logic style main goal was to make the dynamic circuits more robust and with low power dissipation and low delay. Performance analysis of 3 bit Carry Save Adder reveals that proposed logic faster than domino and conventional Carry Save Adder respectively. By the comparison of Dynamic CSA is faster than RCA and CBA. A CSA using conventional logic, domino logic and dynamic logic is designed using Microwind Tool.

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