ISSN XXXX XXXX © 2016 IJESC

Research Article Volume 6 Issue No. 12

Design of Power Efficient 6 Transistor CMOS Full Adder

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Abstract:
Full adders are the most important building blocks in digital design which not only perform addition operations, but also helpful in calculating several other functions such as subtraction, multiplication and division operations. Different types of adders are frequently essential in VLSI technology according to the requirement in processors to ASCIs. In modern research we have found that complementary pass transistor logic (CPL) is much more power efficient than complementary CMOS. In this work describes the power consumption and propagation delay of one-bit CMOS (Complementary MOSFET)full adder, CPL(Complementary pass transistor logic), domain logic full adder and transmission full adder is designed. The actual performance of the circuit can be defined by performing a SPICE simulation. It will be in fared that for transmission gate full adder the parameters like Dynamic and static power consumption and total propagation delay is less, so the transmission gate full adder is much better for use in VLSI technology. This adder will be implemented using S-EDIT, W-EDIT in TANNER tool. With the help of CMOS 018µm technology.

I. INTRODUCTION

Addition is the most commonly used arithmetic operation. It often is the speed limiting element as well. Therefore, careful optimization of the adder is of the utmost importance. This optimization can be proceed either at the logic or circuit level. Typical logic level optimizations try to rear range the Boolean equations so that a faster or smaller circuit is obtained. An example of such a logic optimization is the carry look ahead adder discussed. Circuit optimizations, on the other hand, manipulate transistor sizes and circuit topology to optimize the speed.

Adders are many types. They are

1. Full adder
2. Ripple carry adder
3. Carry look ahead adder
4. Mirror adder
5. Transmission gate adder

2.1 FULL ADDER

A Full Adder (FA) is a logical circuit that performs an addition operation on three binary digits. The full adder produces a sum and a carry value, which are both binary digits. A FA adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as *A*, *B*, and *C*i here *A*, *B* are the operands, and *C*i is a bit carried in (in theory from a past addition by). A and B are the adder inputs, C is the carry input, S is the sum output and Co is the carry output. The Boolean expressions for S and Co are given by

S= AB C + AB C + A C B + ABC (3.1)

Co= AB+BA+CA (3.2)

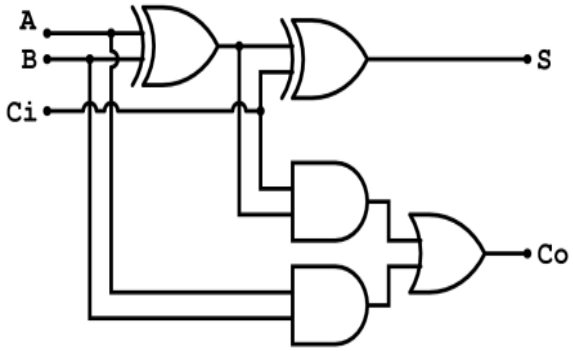

Figure.1. ***Schematic diagram of full adder***

2.2 RIPPLE CARRY ADDER

An n bit adder can be converted by cascading N full adder circuits in series, connecting $Co_{,k-1}$ to $C_{i,k}$ for k=1 to N-1, and the first carry in $C_{i,0}$ to 0. This configuration is called a ripple carry adder, since the carry bit ripples from one stage to other. The delay through the circuit depends upon the number of logic stages that must be traversed and is a function of the applied input signals. For some input signals, no rippling effect occurs at all, while for others, the carry has to ripple all the way from the least significant bit to the most significant bit. The propagation delay of such a structure is defined as the worst case delay over all possible input patterns. In the case of ripple carry adder the worst case delay happens when a carry generated at the least significant bit position propagates all the way to the most significant bit position. This carry is finally consumed in the last stage to produce the sum. The delay is then proportional to the number of bits in the input words N and is approximated by

$$T_{adder} = (N-1)T_{carry} + T_{sum} \quad (3.3)$$

Where T_{carry} and T_{sum} equal the propagation delays from C_i to C_o and S, respectively

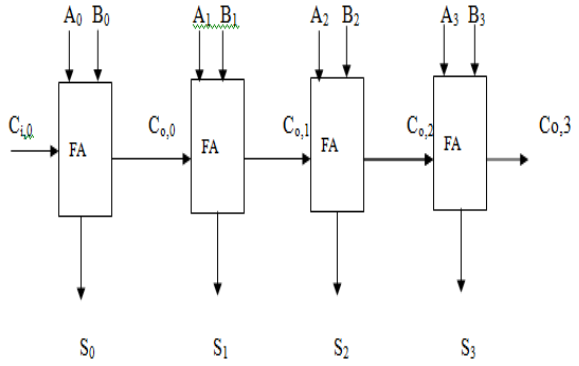

Figure.2. ***Schematic diagram*** **of** ***ripple carry adder***

2.3 CARRY LOOK AHEAD ADDER

The addition of binary numbers in parallel implies that all the bits of and are available for computation at the same time. As in any combinational circuit, the signal must propagate through the gates before the correct output sum is available. The output will not be correct unless the signals are given enough time to propagate through the gates connected form the input to the output. The longest propagation delay time in an adder is the time it takes the carry to propagate through the full adders. The signal form the carry input Ci to the output carry Ci+1 propagates through an AND gate and an OR gate, which equals 2 gate levels.

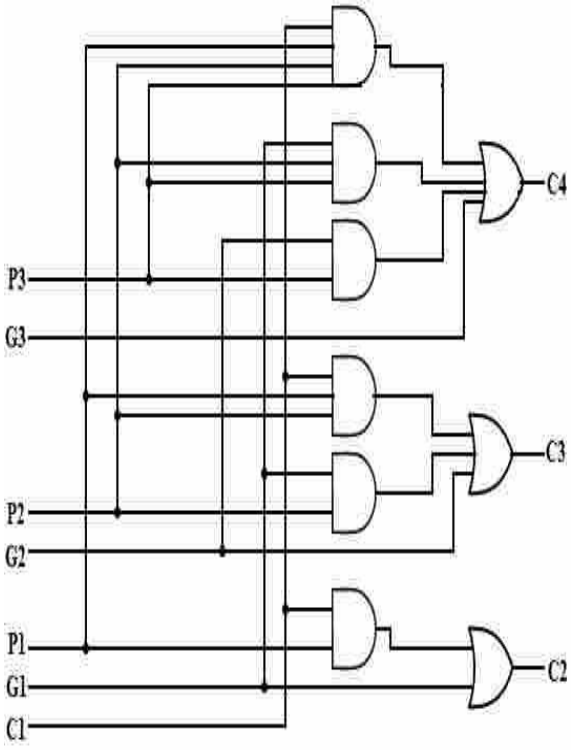

Figure.3. ***Logic Diagram for Carry Look ahead Generator***

The construction of a four-bit adder with a carry look ahead scheme is the following:

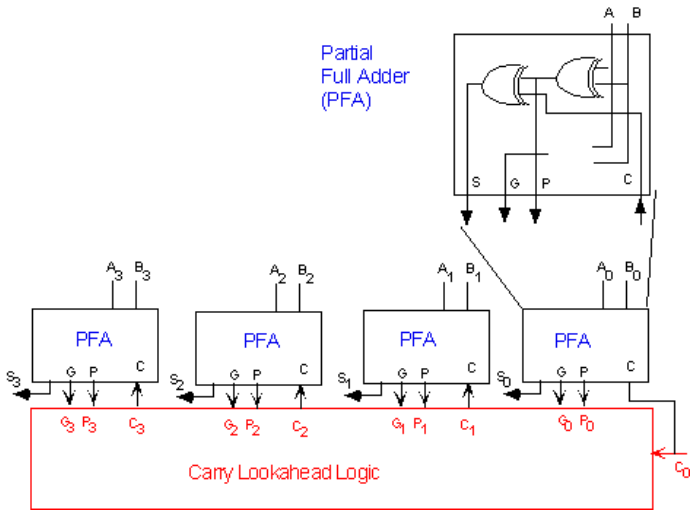

Figure.4. ***Schematic diagram for carry look ahead adder***

2.4 MIRROR ADDER

An improved adder circuit, also called the mirror adder, is shown in Figure 11-6. Its operation is based on Eq.(11.3). this carry-generation circuitry is worth analyzing. First, the carry-inverting gate is eliminated, as suggested in the previous section. Secondly, the PDN and PUN networks of the gate are not dual. Instead, they form a clever implementation of the propagate/generate/delete function- when either D or G is high, C_0 bar is set to V_{DD} or GND, respectively. When the conditions for a propagate are valid (or P is 1)[3], the incoming carry is propagated (in inverted format) to C_0bar. This results in a considerable reduction in both area and delay. The analysis of the sum circuitry is left to the reader. The following observations are worth considering. This full-adder cell requires only 24 transistors.

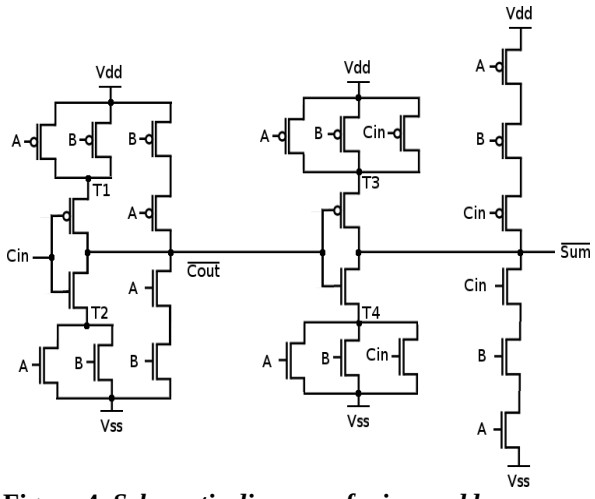

Figure.4. ***Schematic diagram of mirror adder***

2.5 TRANSMISSION GATE ADDER

A full adder can be designed to use multiplexers and XORs. While this is impractical in a complementary CMOS implementation, it becomes attractive when the multiplexers and XORs are implemented as transmission gates. A full adder implementation based on this approach is shown in figure and uses 24 transistors. It is based on the probate- generate model,

introduced in the propagate signal, which is the XOR of inputs A and B, is used to select the true or complementary value of the input carry as the new sum output. Based on the propagate signal, the output is either set to the input carry, or either one of inputs A or B. One of interesting features of such an adder is that it has similar delays for both sum and carries outputs.

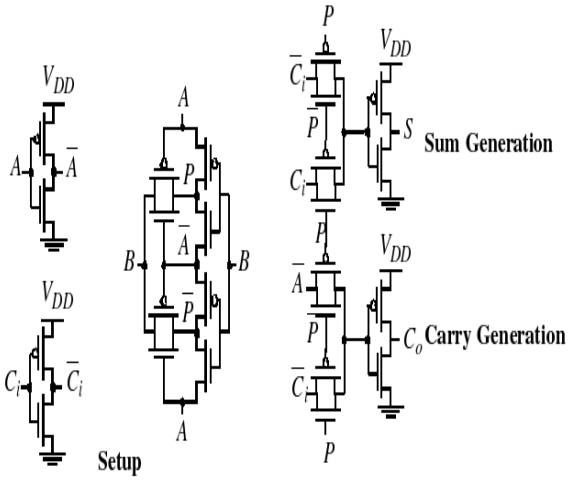

Figure.5. ***Transmission gate adder***

III.EXISTING METHOD:

3.1 FULL ADDER

Full adder is the combinational circuit that performs addition of three bits. It consists of three inputs a,b,c and two outputs sum and carry.

3.1.1SCHEMATIC DIAGRAM OF CMOS FULL ADDER

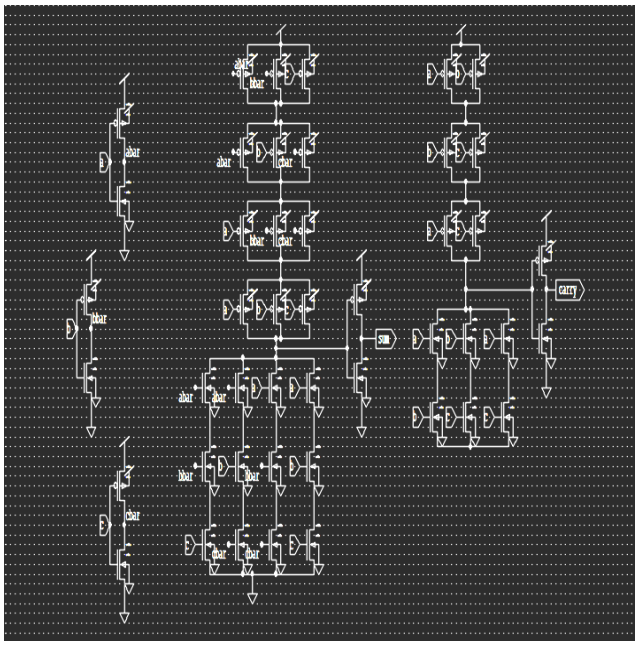

Figure.6. ***Schematic diagram of full adder***

3.1.2 SYMBOLIC DIAGRAM OF CMOS FULL ADDER

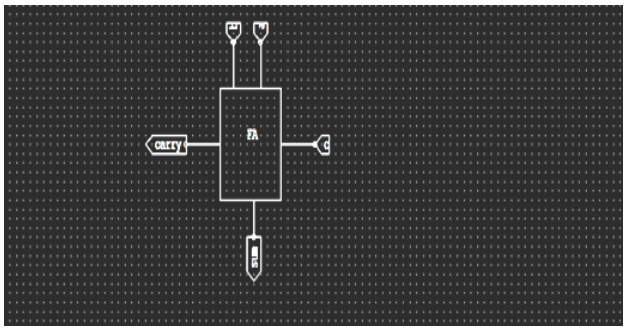

Figure.7. ***Symbolic Diagram of Full Adder***

3.2 4 BIT RIPPLE CARRY ADDER

A Ripple Adder can be constructed with full adders connected in cascade with the output carry from each full adder connected to the input carry of the next full adder in the chain.

3.2.1 SCHEMATIC DIAGRAM OF 4 BIT RIPPLE CARRY ADDER

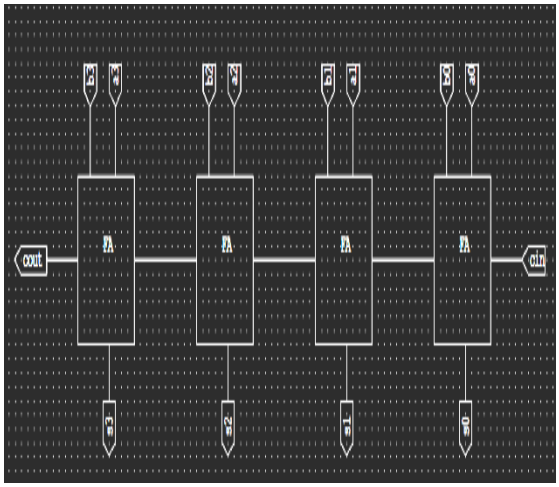

Figure.8. ***Schematic diagram of 4 bit ripple carry adder***

3.2.2 SYMBOLIC DIAGRAM OF 4 BIT RIPPLE ADDER

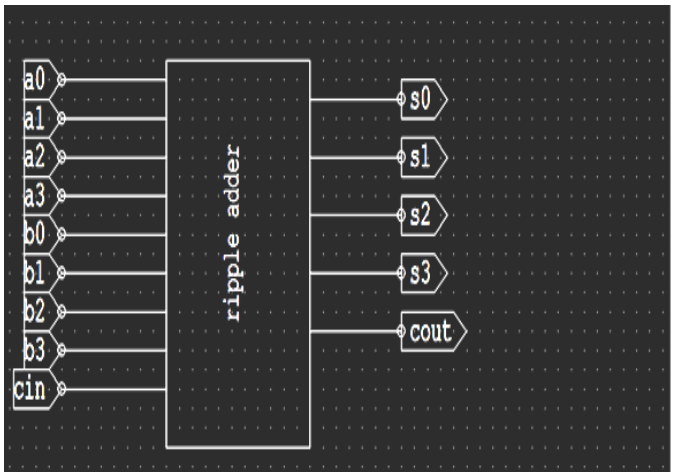

Figure.9. ***Symbolic diagram of 4 bit ripple carry adder***

3.3 CARRY LOOK AHEAD ADDER

3.3.1 SCHEMATIC DIAGRAM OF CARRY LOOK AHEAD ADDER

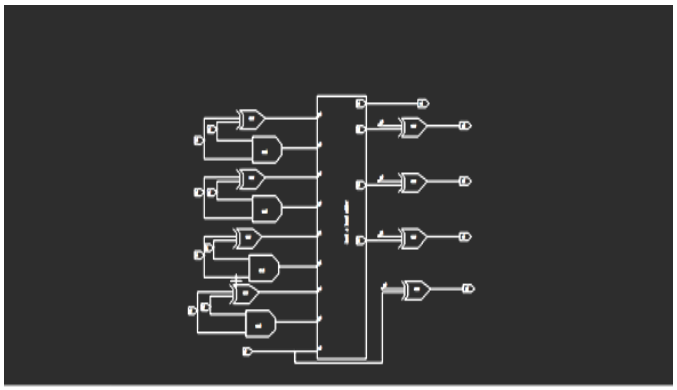

Figure.10. ***Schematic diagram of carry look ahead adder***

3.3.2 SYMBOLIC DIAGRAM OF CARRY LOOK AHEAD ADDER

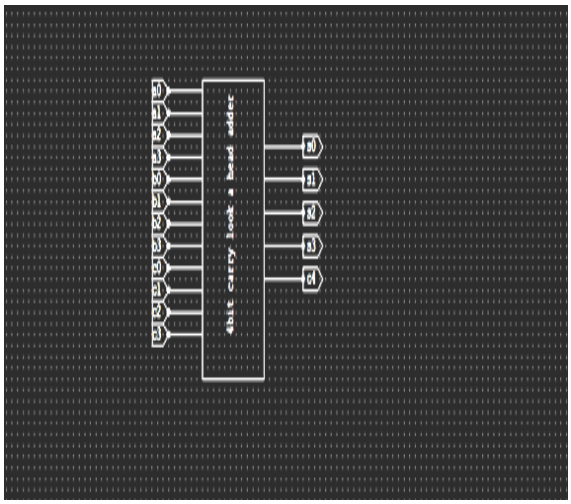

Figure.11. ***Symbolic diagram of carry look ahead adder***

3.4 4 BIT MIRROR ADDER

3.4.1 SCHEMATIC DIAGRAM OF 4 BIT MIRROR ADDER

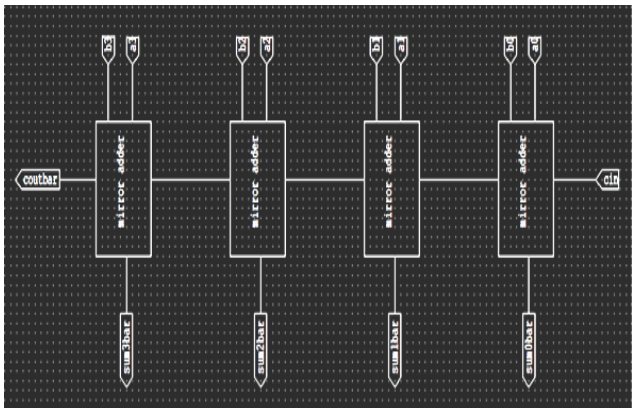

Figure.12. ***Schematic diagram of 4 bit mirror adder***

3.4.2 SYMBOLIC DIAGRAM OF 4 BIT MIRROR ADDER

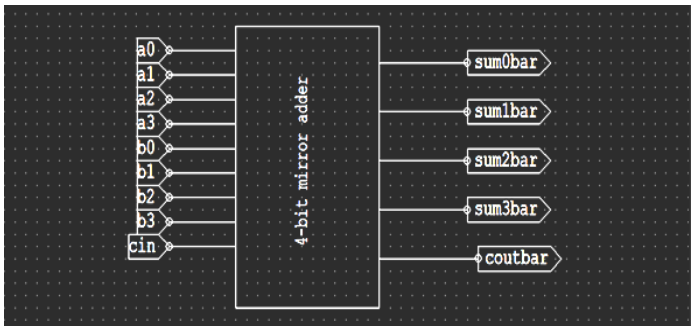

Figure.13. ***Symbolic diagram of 4 bit mirror adder***

3.4.3. MIRROR ADDER

3.4.4 SCHEMATIC DIAGRAM OF MIRROR ADDER

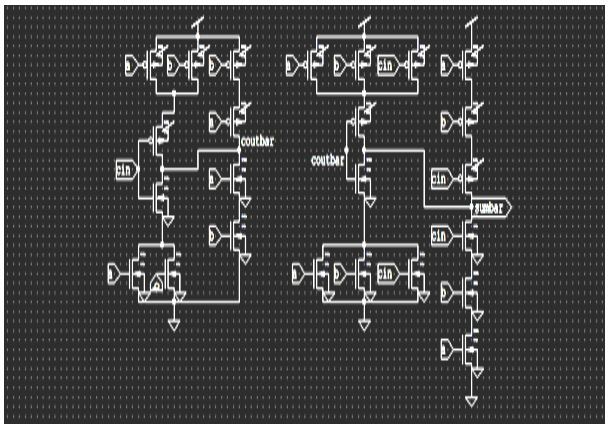

Figure.14. ***Schematic diagram of mirror adder***

3.4.5 SYMBOLIC DIAGRAM OF MIRROR ADDER

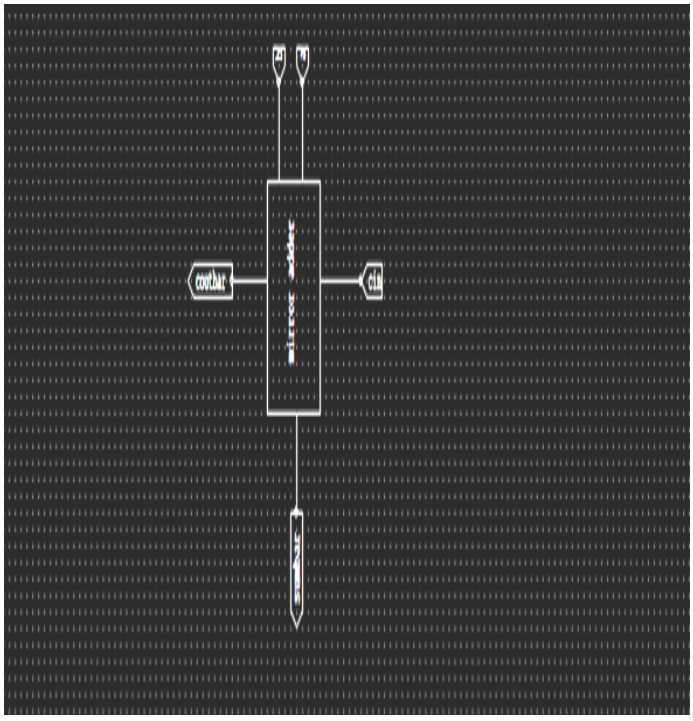

Figure.15. ***Symbolic diagram of mirror adder***

3.5 4 BIT TRANSMISSION GATE ADDER

3.5.1 SCHEMATIC DIAGRAM OF 4 BIT TRANSMISSION GATE ADDER

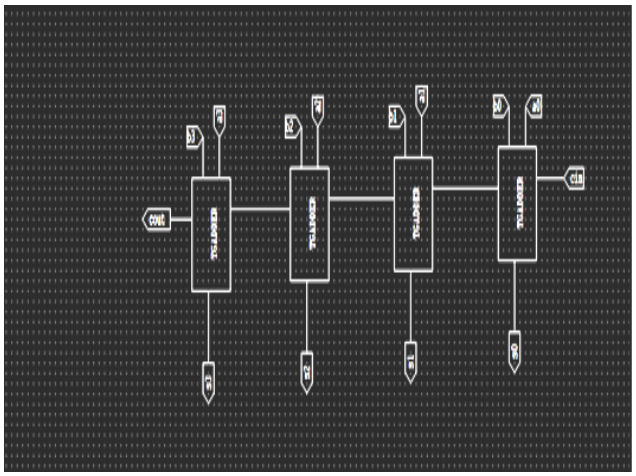

Figure.16. ***Schematic diagram of 4 Bit transmission gate adder***

3.5.2 SYMBOLIC DIAGRAM OF 4 BIT TRANSMISSION GATE ADDER

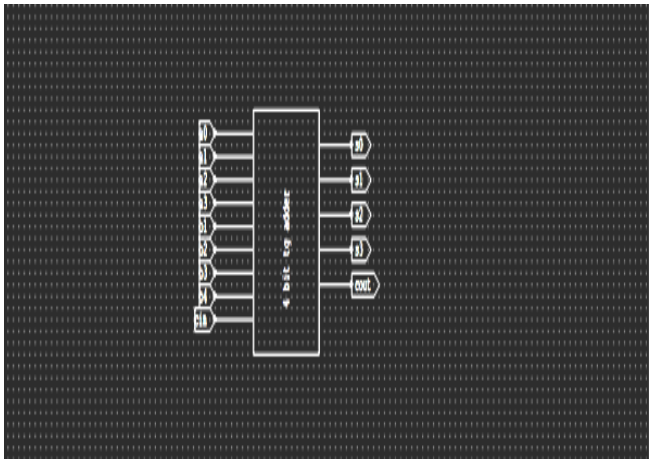

Figure .17. ***Symbolic diagram of 4 bit transmission gate adder***

3.5.3 TRANSMISSION GATE ADDER

3.5.4. SCHEMATIC DIAGRAM OF TRANSMISSION GATE ADDER

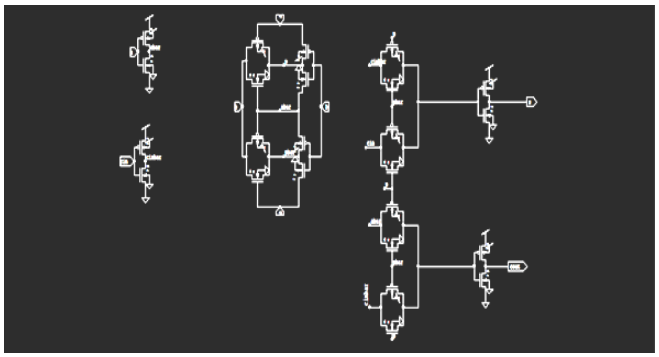

Figure.18. ***Schematic diagram of transmission gate adder***

3.5.5 SYMBOLIC DIAGRAM OF TRANSMISSION GATE ADDER

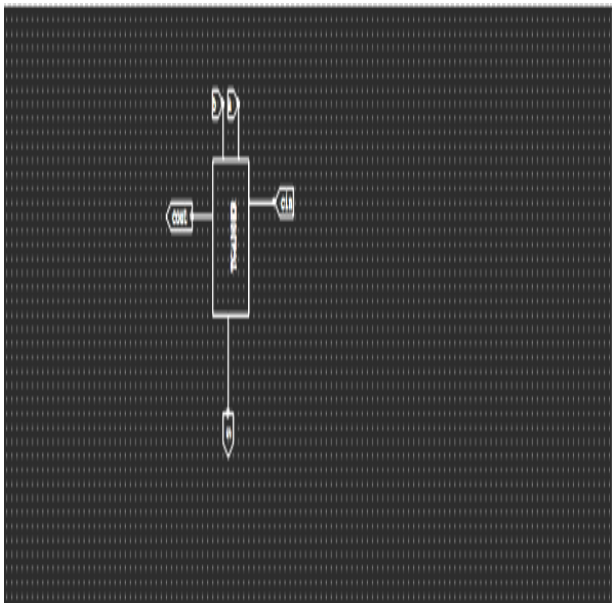

Figure.19. ***Symbolic diagram of transmission gate adder***

IV. PROPOSED METHOD

6 Transistor

Using Multiple Valued Logic (MVL) have potential advantages in chips performing extensive arithmetic operations due to the reduction in the number of MOS transistors and relaxed wiring requirements due to the smaller word size . The MVL is a potential alternative to Binary logic . Reducing the amount of interconnects and the number of active devices on a given chip . By extending MVL off-chip, we can also reduce chip pin out. These reductions can improve performance in terms of speed, area and power dissipation. The MVL circuits are generally operated in two modes of voltage or current. Current Mode Logic (CML) has some advantages over voltage mode MVL. Implementing voltage-mode MVL requires partitioning the total voltage range, zero to supply voltage in to many discrete levels. Thus, the dynamic range and the noise margin are highly dependent on the supply voltage. In current-mode circuits, currents are usually defined to have logical levels that are integer multiple of a reference current unit. Current can be copied, scaled and algebraically sign-changed with a simple current mirror. The frequently used linear sum operation can be performed simply by wiring, resulting in a reduced number of active devices in the circuit. Using current instead of voltage as the alternating parameter is possible. Of course the designing of circuits should be in another way. One of the most important arithmetic operations in computer arithmetic is addition. For implementing any other arithmetic operation such as subtraction, multiplication or even logarithmic function we need efficient adders. In recent years several variations of3-valued and 4-valued circuits have been defined for implementing 2-input and 3-input adders with Borrow/carry save redundant number representation, which is the number representation used in . They are based on 3-valued to binary converter (3-BC) and 4valued to binary converter (4-BC) circuits. These circuits are fundamental ones. Moreover, as we will detail, the 4-BC cell is the current-mode binary full adder. The paper begins with a

discussion of four valued CML circuitry for one bit adder followed by a description of MVL current mode circuits. Then the implementation of current mode circuits and its related problems are discussed and finally the proposed six transistor adder based on MVL method is introduced. The proposed 6T full adder sum is generated using 2T XOR module twice, and carry is generated using NMOS and PMOS pass transistor logic devices.

The equations for 6T full adder design are:

SUM=(a xor b) cbar+ (a xor b)bar c (5.1)

CARRY=(a xor b)bar a + (a xor b)c (5.2)

In this design (a xor b) signal is passed to the pass transistor multiplexer made of two transistors to choose one among two. To generate carry (a xor b) is sent to multiplexer to choose between a, c. and to generate sum (a xor a) is sent to choose between c`, c.

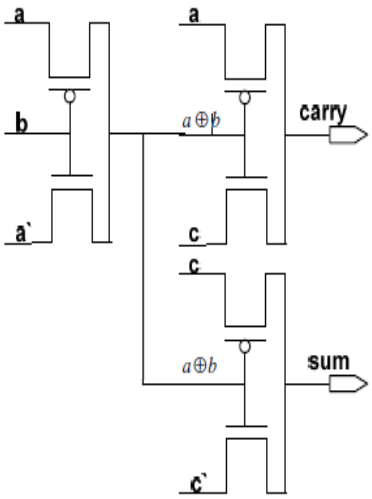

Figure. 20.1. ***6 transistor adder***

4. 1 SCHEMATIC DIAGRAM OF 6 TRANSISTOR ADDER

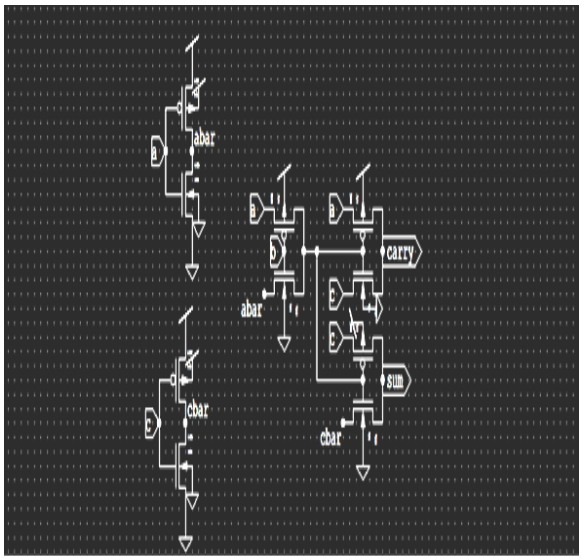

Figure.21. ***Schematic diagram of 6 transistor***

4.2 SYMBOLIC DIAGRAM OF 6 TRANSISTOR ADDER

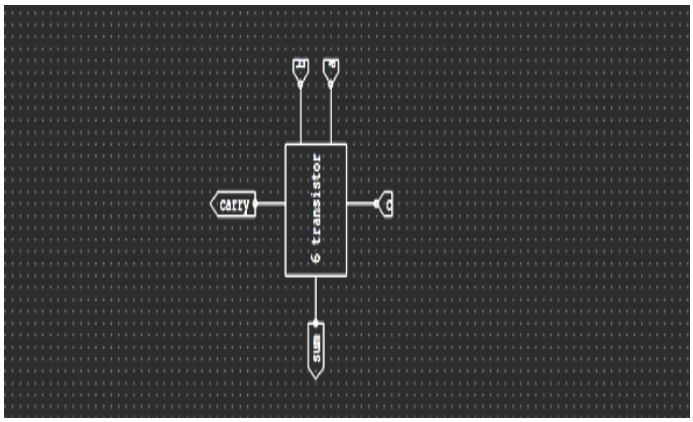

Figure.22. ***Symbolic diagram of 6 transistor adder***

4.3 4 BIT 6 TRANSISTOR ADDER

Example:

1 0 1 0
1 0 1 0
0 1 0 0
Carry=1

4.3.5 SCHEMATIC DIAGRAM OF 4 BIT 6TRANSISTOR ADDER

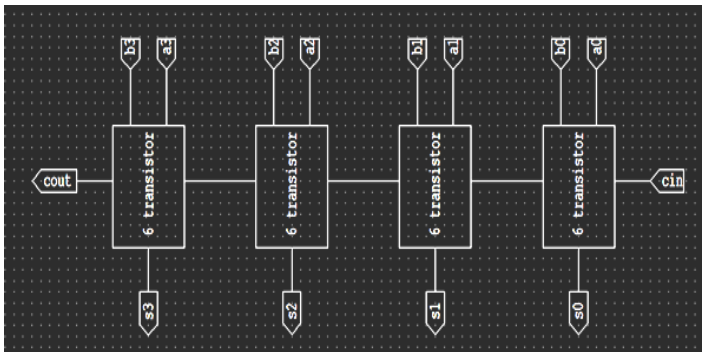

Figure.23. ***Schematic diagram of 4-bit 6 transistor adder***

4.3.6 SYMBOLIC DIAGRAM OF 4 BIT 6 TRANSISTOR ADDER

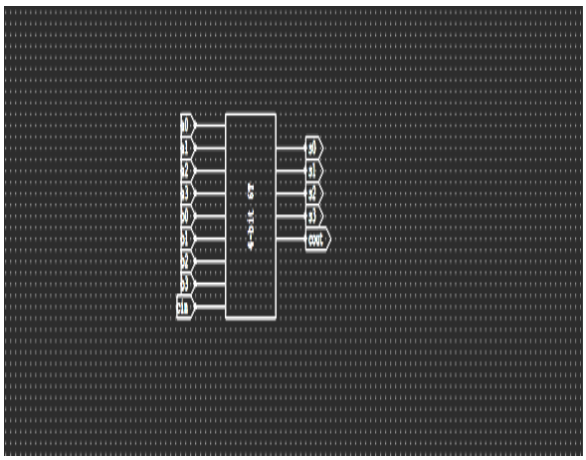

Figure.24. ***Symbolic diagram of 4 bit 6 transistor adder***

V. SIMULATION

5.1. WAVE FORMS OF 4 BIT 6 TRANSISTOR ADDER

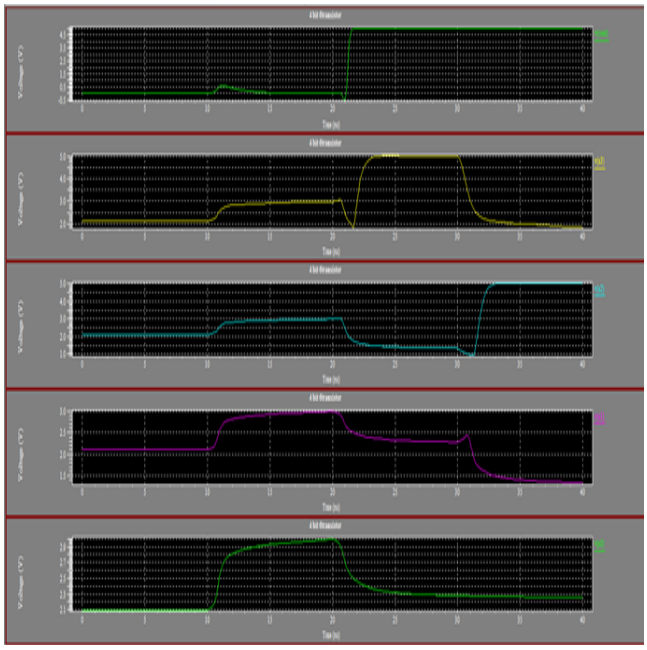

Figure.25. ***Wave forms of 4bit 6transistor adder***

POWER:

```
Power Results
v1 from time 1e-009 to 4e-008
Average power consumed -> 1.021877e-003 watts
Max power 1.009077e-002 at time 3.09194e-008
Min power 4.266466e-007 at time 2.48081e-008


* END NON-GRAPHICAL DATA

* Parsing                          0.03 seconds
* Setup                            0.01 seconds
* DC operating point               0.01 seconds
* Transient Analysis               0.07 seconds
* ----------------------------------------
* Total                            0.12 seconds
```

AREA:

```
Device and node counts:
          MOSFETs - 40              MOSFET geometries - 2
             BJTs - 0                        JFETs - 0
           MESFETs - 0                       Diodes - 0
        Capacitors - 0                    Resistors - 0
         Inductors - 0                Mutual inductors - 0
Transmission lines - 0       Coupled transmission lines - 0
   Voltage sources - 10                Current sources - 0
              VCVS - 0                          VCCS - 0
              CCVS - 0                          CCCS - 0
  V-control switch - 0              I-control switch - 0
     Macro devices - 0       Functional model instances - 0
       Subcircuits - 2            Subcircuit instances - 12
 Independent nodes - 21                Boundary nodes - 11
       Total nodes - 32
```

Table .1. ***Power and Area analysis of adders***

TYPES OF ADDERS	NO.OF TRANSISTORS	POWER CONSUMED
FULL ADDER	46	1.783369e-0.03 watts
RIPPLE CARRY ADDER	184	9.501665e-003 watts
CARRY LOOK AHEAD ADDER	136	1.720919e-0.02watts
MIRROR ADDER	96	2.512592e-0.03 watts
TRANSMISSION GATE ADDER	96	3.195777e-0.03 watts
6 TRANSISTOR ADDER	40	1.021877e-0.03 watts

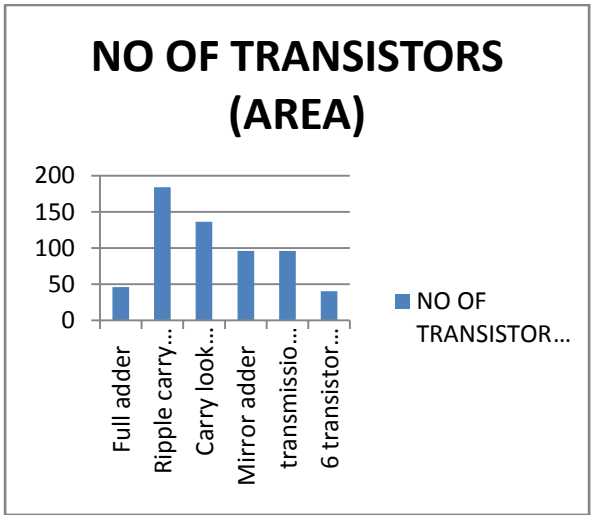

Figure.26. ***Bar graph representation of adders for area***

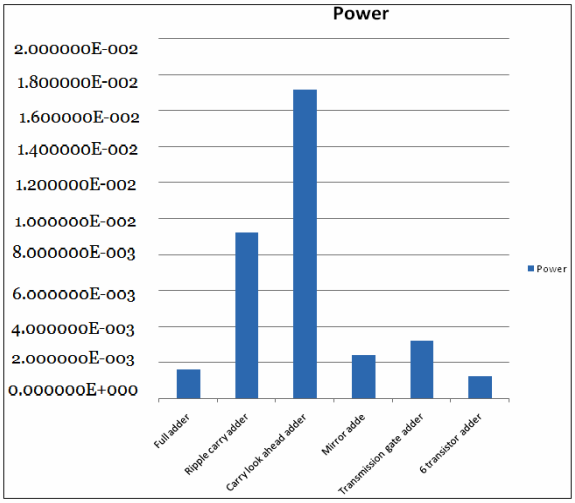

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Figure.27. ***Bar graph representation of adders for power***

VI. CONCLUSION

In this work we designed and implemented different types of adder using Tanner tools withC MOS 018µm technology. Performance of those adder are analysed with the help of W-Edit through simulation. In this work various adders like CMOS full adder Ripple carry adder, Carry Look Ahead adder, Transmission

gate adder, Mirror adder and a novel 6T adder have been simulated and synthesized with the help of SPICE net list and their power results are obtained. Finally they obtained results like power and area are compared for 4-bit adder. From the table 6T adder is the efficient adder with respect to area and power for the application of ALU operations.

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