ISSN XXXX XXXX © 2019 IJESC

Research Article Volume 9 Issue No.3

Digital Lock System using FSM

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Abstract:
Finite State Machine is the main controller used in digital lock system. The function of that controller is to detect the correct input sequence. The correct number of input bits is only known to the person who sets the password. This responds only to the right sequence of input bits. The digital lock system opens only when required number of input bits entered is correct .If the input bits entered is not correct then the lock will automatically reset .The lock will reset upto three attempts to unlock the door. After three wrong attempts if an unknown user tries to enter the password then the authorized used will be indicated using an alarm.

I. INTRODUCTION

Communication network mostly use digital data to be transferred because digital data will give more accuracy than analog data .Digital data is transmitted in form of bits at high speed.The transmitting bits is called as stream of bits. The end user can receive only the required information.The digital lock system unlock the lock if correct binary code is entered.The main purpose of this system is to provide more security features. The mechanical locks are easily broken.If digital locks are used it eliminates that disadvantage .The another advantage involved in this is binary digits are entered as inputs.Normally numerical or alphanumeric method is used as inputs. FSM are commonly a sequential logic circuit. Systems need to realize a specific sequence can us FSM as their controller In this digital system we have used Moore machine.Although it suffers disadvantage of having more number of sates,its main advantage is producing a stable outputs which is not possible in Mealy machine .The Simulation is done using Model Sim Software whose output is also discussed..

II. DESIGN FLOW

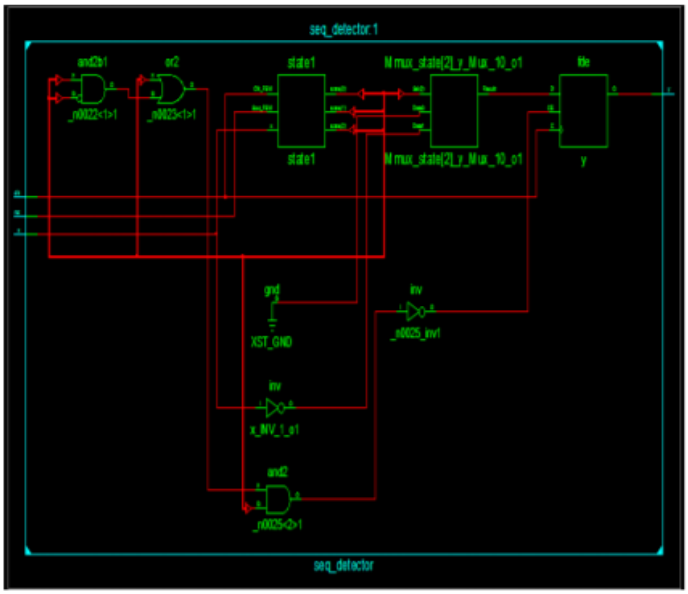
The procedure of this system is based on the detection of binary number in correct order.In order to unlock the system one has to enter the correct password using given module. This kind of lock can avoid the problems caused by the copying of keys.The keyless based digital lock system provides more security than mechanical locks.Nowdays more number of facilities have been used like fingerprint based, electronic lock etc. For example the code used to unlock is “1011”. The inputs to be considered are clk,reset,enter,set,idle and the output to be considered are out and buzzer.The out indicates the unlocking status.The buzzer is used as an indication signal if more than 3 attempts taken.

The unlocking is considered by making the output bit as “1” as the correct pattern is fed in the input.Due to the usage of Moore machine in this system it provides stable output at all times.Its main advantage is the input password bits is only known to the authorized users.In normal cases unauthorized users have major advantage of hacking the password and easily unlock the door. The above disadvantage is cleared by using digital lock system using Finite State Machine. The binary input bits used as password is also a another advantage of this system.

III. RTL SYNTHESIS

Most of the hardware designers use HDL to describe the designs. The advantage of HDL is that it can be used for different levels of abstraction. HDL is a high level programming language, with programming constructs such as assignments, conditions, iterations and extensions for timing specification, concurrency and data structure proper for modelling different aspects of hardware. To describe the behavior of any digital system two languages are mostly used

1.VERILOG HDL
2.VHDL



RTL SCHEMATIC OF SYSTEM

HDL supports features like development, verification, synthesis and testing of the hardware systems .In this system we have used Verilog as the language. The type of encoding needs to be chosen correctly. The binary style is implemented in this design. Synthesis is the process of automatic hardware generation from a design description that has an unambiguous hardware correspondence. Synthesis eliminates all the time constraints file handling and other constructs that don’t transfer to sequential or combinational circuits. Conversion of higher level to gate level is done by using synthesis tools. Verilog constructs used in an RT level design are procedural statements, continuous statements and instantiation statements

IV. RESULTS AND DICUSSIONS

CLOCK
Clock signal is a signal that oscillates between high and a low state.Circuits using clock signal for synchronization may become active at either rising edge or falling edge.The different path of the signals can be synchronized using clock signal.

RESET
Reset function is normally included in digital circuits ignored to bring the logic to known state.It is mostly required for the control logic and may be eliminated from data path logic reducing logic area.

SET
Set signal is like an enable signal which can be used to updates the output only when this control signal is made high.If the control signal is not set as high then the output cant be updated.

ENTER
Enter is used in order to type the password after it is set.

CURRENT AND NEXT STATE
The current and next state signals can be changed according to the required pattern detection.It may also be depend on the type of design used for digital circuits.

TRIAL
Trial signal is used to define the condition used.The number of trial bits can be defined by the user.

OUT AND BUZZER
The out and buzzer may be changed according to inputs given and the conditions given in the design.

5.2 SIMULATION OUTPUT

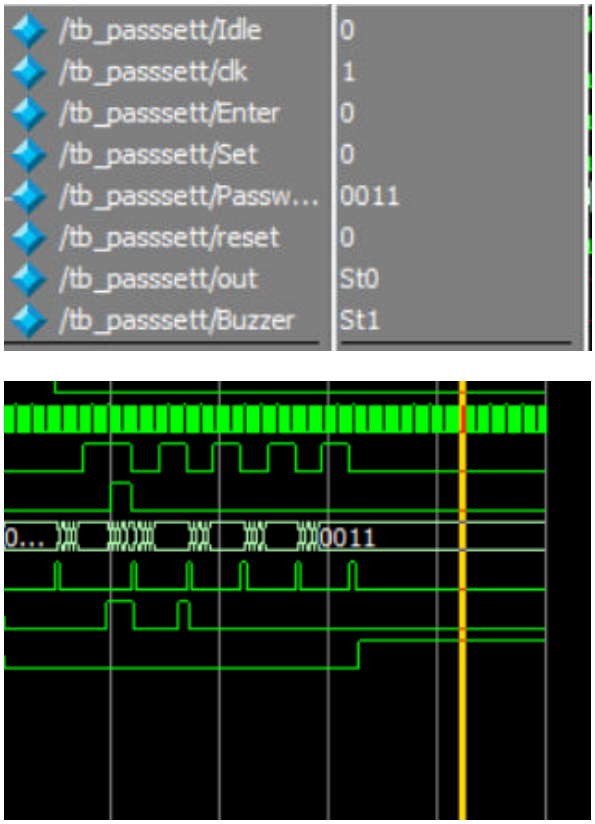


Figure.1. Simulation output

5.3 STEPS INVOLVED IN SIMULATION

CHECKING WHETHER SYSTEM IS IDLE

At first the system check whether it is idle or not.If it is idle and set bit is higher than the required password is set at posedge clock.

PASSWORD ENTRY
After setting the password when they enter bit is high, then the unknown user can type the password.If the password is correct the lock will be opened which will be indicated using out signal.

TRIAL CHECKING
If the password entered by the unknown user is not correct then next chance will be given using the reset signal .The reset signal avoids the wrongly entered password and gives another attempt.

BUZZER OUTPUT
After three wrong attempts the user will be indicated using an alarm.This is made by using buzzer signal as the output.

RESETTING THE PASSWORD
The predefined password is again reset using set signal which is the main signal used in the simulation.After the new password being chosen if the older one is given as password it will not be detected by the system.The bits to be set as password is decided by user which will not be known to the unknown user is the major advantage in this digital lock system. In the Verilog coding, the test module generates a 10 Hz clock using an initial sequential block-coding. The whole digital lock system provides a secured architecture and without knowing the correct password sequence, it is impossible to open it. In every wrong entry, the system goes in a locked state and an alarm occurs. However, if the total power loss of the system occurs, then it will go in the locked state and in that time nobody can open it. To solve this problem, an internal battery connection is required to activate the system during power failure. Simulation for design validation is done before a design is synthesized. This simulation pass is also called as behavioral simulation.

V. CONCLUSION AND FUTURE SCOPE

Security is the art of restricting admittance to certain entities and is a huge concern for our global society.So in this project we present the FSM based security lock system with the help of Model Sim Software. The design is verified or tested by the software and used in many applications. Finally the functional verification has been carried out with proper analysis of the output data. The simulated output signifies the proper functioning of the system. In future, changing the code of the lock can be considered as open research issue. The only thing to do is to implement it in the hardware and make use of it. Thus digital lock system is further modified into applications like automatic door close system in office.It can also used in automatic door lock system in houses,cars and offices .This is mainly used where fixed time slot or fixed duration is required.It can be used in remote interface which give a more reliable program.It is also used in many industrial applications .By adding video camera ,this can be used as low cost home security system for apartments. The above digital lock system is very efficient in terms of speed and time.

VI. REFERENCE

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