# Power Quality Improvement of PV Power Generation Systems using Solid State Transformer

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**Abstract:**
A three phase Solid State Transformer (SST) based on serial H-Bridge multilevel converter, with favorable circumstances as expandable secluded structure, controlled power quality and low reliance on copper/steel, is applied to replace the conventional line frequency step up transformer on PV generation. In view of the input parallel output serial Dual Active Bridge (DAB) based sub modules with internal dc links, the voltage adjust of medium voltage (MV) dc links and the control of low voltage side input dc links are concerned. A new control scheme is proposed based on the voltage tracking control of DC links, inside which the voltage adjust between sub modules is acknowledged through average voltage control and dc link voltage tracking control. Improvements are also proposed for shaping DAB current and increasing the speed of dynamic response. Simulation results are presented at the end.

**Keywords:** Solid State Transformer, Power Electronics Transformer, Control of SST, Cascaded Converter, Dual Active Bridge.

## I. INTRODUCTION

Conventional consolidated three phase inverters for photovoltaic (PV) generation utilize step-up line frequency (LF) transformers to connect the distribution system. The LF transformer has undesirable properties as bulky construction with large amount of metal (copper/steel) and power quality susceptibility. In contrast, the solid state transformer (SST), with medium frequency (MF)/ high frequency (HF) transformers and MF/HF switching devices not only performs voltage step, but can also provide much higher power density with less metal material and improved power quality, which is proper for PV generation. To eliminate the LF transformer, without high voltage rating devices, the feasible high-voltage high-power SST have to turn to multilevel topology and commercial available low-voltage devices. [1, 2, 3]. In this paper as shown in Fig.1, utilized in PV generation, a three phase SST with low-voltage dc input and medium-voltage ac output is based on the concept of serial H-bridge multilevel converter. A DAB and an H-bridge cascaded with it through MV dc link constitute a sub module (SM), whose input port is the dc input of the DAB, and the output port is the ac output of the H-bridge. The DAB converter with MF transformer is selected because of its high power density, zero voltage switch (ZVS) and fast dynamic response [4]. For the voltage step-up function, SMs are composed to input-parallel output-serial (IPOS) structure. The parallel input ports produce a low voltage (LV) dc link connected to DC-DC PV array adaptors, and the output ports form three serial strings connected with distribution grid through reactors. For the MV high power PV generation to three-phase distribution system using minimum number of SMs, the three serial strings of output ports of SMs are organized into wye connection. Much concern focused on how to maintain the voltage and voltage balance of MV dc links for safety and stability. In reference [3, 5], the phase shift modulation method is applied in DABs, and the LV dc link voltage is controlled by regulating all DABs with a same phase shift angle. Because of the parameter difference between

submodules, the power delivered by DABs differs, leading to voltage unbalance. A trimming scheme for the modulation signal of H-bridges is
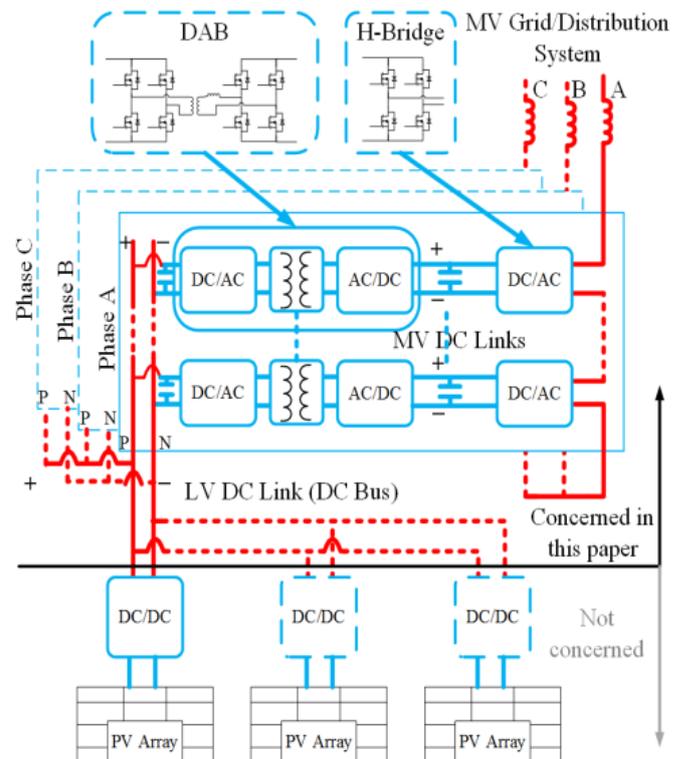


**Figure 1. Design of a three phase sst for pv generation**

Applied to balance the voltages of MV dc links. The DAB power unbalance is solved in [5] and [6]. Different from PI regulation, in [7] the MV dc link voltages are balanced by a modulation method of the serial seven-level converter. In [8], for the single-phase SST, only the SPWM of #1 submodule is determined by a voltage close loop which directly maintains the MV dc link voltage of #1 submodule, and the voltages of

all MV dc links are controlled to track the LV dc link. As a result, the voltages of all MV & LV dc links are indirectly determined by the voltage close loop in #1 submodule. A master-slave control scheme is proposed in [9]. The slave SMs receive gate signals from the sole master SM, bringing unbalanced power &voltage because of parameter differences. Compensation schemes are developed to solve the unbalance. In section II, the analysis model of three-phase SST in PV generation is shown and an overall control scheme is given; In section III, improvements for MV dc link voltage tracking control are proposed; In section IV, simulation results are shown

## II. MODELING AND THE VOLTAGE CONTROL SCHEME OF DC LINKS

### A. Modeling of the SST

The diagram of a SST for PV generation with variable definitions are shown in Fig.2. Dynamic functions are shown from (1) to (3), where complementary switch states of $Q_1$ and $Q_2$ in SM_ij are $s_{1\_ij}$ and $s_{2\_ij}$ respectively (i = a, b or c for phase, j for the sequence in phase i), while complementary switch states $s_{3\_ij}$ and $s_{4\_ij}$ are of $Q_3$ and $Q_4$ respectively.

$$s_{n\_ij} = \begin{cases} 1, & \text{When device Qn of submodule ij is on;} \\ 0, & \text{When device Qn of submodule ij is off.} \end{cases} \quad (1)$$

$$\begin{cases} L\dfrac{d}{dt}(i_a - i_b) + R(i_a - i_b) = \sum_j u_{aj} - \sum_j u_{bj} - u_{AB} \\ L\dfrac{d}{dt}(i_b - i_c) + R(i_b - i_c) = \sum_j u_{bj} - \sum_j u_{cj} - u_{BC} \\ L\dfrac{d}{dt}(i_c - i_a) + R(i_c - i_a) = \sum_j u_{cj} - \sum_j u_{aj} - u_{CA} \\ u_{ij} = s_{1\_ij}u_{DCM\_ij} - s_{3\_ij}u_{DCM\_ij} \end{cases} \quad (2)$$

$$\begin{cases} C_{MV}\dfrac{d}{dt}u_{DCM\_ij} = i_{DAB\_out\_ij} - i_{dc\_ij} \\ i_{dc\_ij} = s_{1\_ij}i_i - s_{3\_ij}i_i \end{cases} \quad (3)$$

$$\frac{1}{2}\left(\sum_{ij}C_{LV}\right)\frac{d}{dt}u_{DCL}^2(t) = p_{in}(t) - \sum_{ij}p_{DAB\_ij}(t) \quad (4)$$



**(a)**
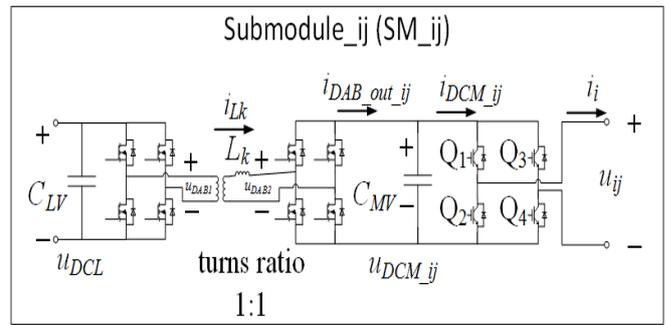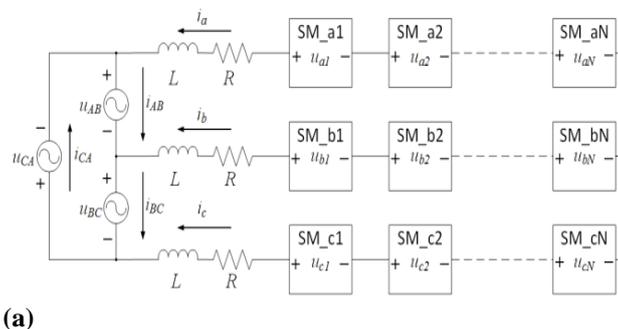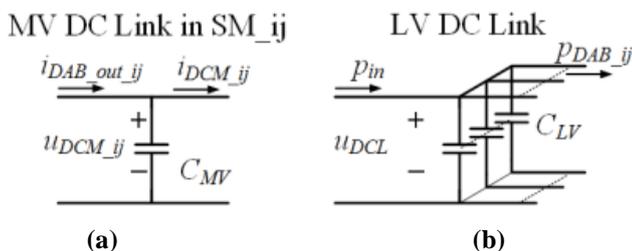




**(b)**
**Figure.2. SST diagram and variable definitions.(a) Three-phase serial H-bridge multilevel structure; (b) Submodule principle. Input ports on CLV are parallel.**
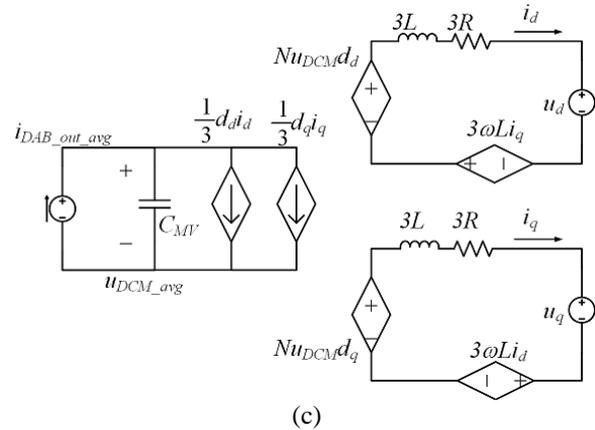


**(c)**
**Figure. 3. SST analysis model.**

The analysis model of a SST for PV generation and variable definitions in this paper are shown in Fig.3. Dynamics of MV dc link voltage $u_{DCM\_ij}$ and LV dc link voltage $u_{DCL}$ are shown in (3) and (4) respectively, variables defined in Fig.3 (a) and (b). The power delivered by DAB, $p_{DAB\_ij}$, is calculated in (5), where $\Phi ij$ is the phase shift angle, and $fsw$ is the switch frequency. The switch cycle average model in d-q coordinates are derived in (6) and (7), and a graphical description is depicted in Fig.3 (c).

$$p_{DAB\_ij} = \frac{u_{DCL}u_{DCM\_ij}\phi_{ij}(\pi - \phi_{ij})}{2\pi^2 f_{sw}L_k} \quad (5)$$

The switch cycle average model in d-q coordinates are derived in (6), and if all the MV DC link voltages ($u_{DCM\_ij}$) are balanced and equals to $u_{DCM}$, (6) is also derived. Relation between average voltage of MV dc links and output AC current in d-q-0 coordinates is revealed by (7).

$$3L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + 3L\begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + 3R\begin{bmatrix} i_d \\ i_q \end{bmatrix} = Nu_{DCM}\begin{bmatrix} d_d \\ d_q \end{bmatrix} - \begin{bmatrix} u_d \\ u_q \end{bmatrix} \quad (6)$$

$$\begin{cases} C_{MV}\dfrac{d}{dt}u_{DCM\_avg} = i_{DAB\_out\_avg} - \dfrac{1}{3}(d_di_d + d_qi_q) \\ u_{DCM\_avg} = \dfrac{1}{3N}\sum_{i,j}u_{DCM\_ij} \\ i_{DAB\_out\_avg} = \dfrac{1}{3N}\sum_{i,j}i_{DAB\_out\_ij} \end{cases} \quad (7)$$

## B. The Voltage Control Scheme of DC Links

The inner d-q current control and voltage control of dc links are shown in Fig.3. As identified in (4), it is convenient to regulate id to control the average of all MV dc link voltages, because of the simplified control object: integrator. Regulation scheme of d-q current is designed similarly to traditional three phase inverter according to (5). Carrier-phase-shift (CPS) PWM is used to drive the IGBT gates of serial H-bridge inverters. Based on dynamics depicted in (6) and (7), the control scheme that MV dc link voltage $u_{DCM\_ij}$ tracks LV dc link voltage $u_{DCL}$ is shown in Fig.4 (b). In reference [8] the average power close loop is used within MV dc link voltage control, which requires much higher sample frequency than switch frequency. Another way here to simplify the control structure and reduce stress of sample frequency, $u_{DCM\_ij}$ is controlled by directly regulating phase angle $\Phi ij$ of phase shift modulation (PSM in Fig.4 (b)).
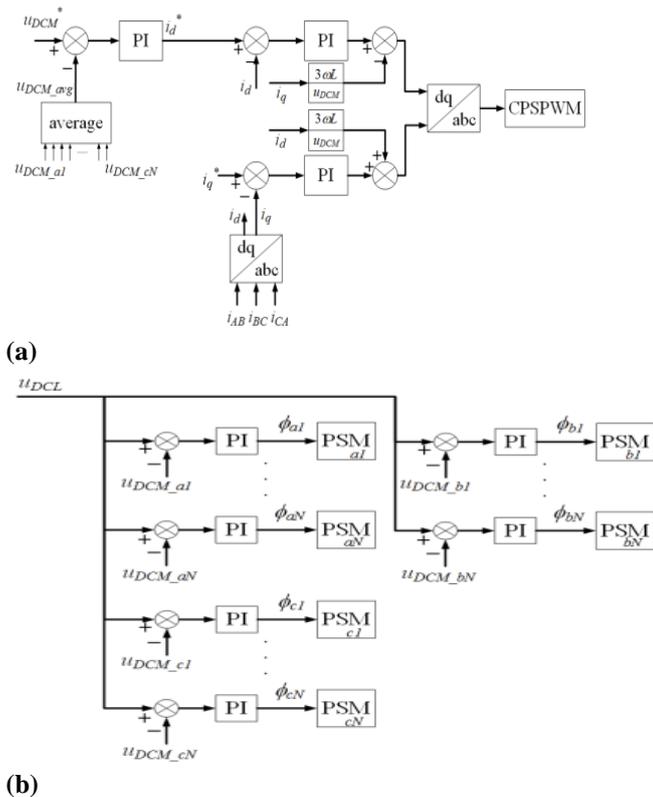


**(a)**



**(b)**

**Figure.4. the proposed overall control scheme of SST. (a) id, iq regulation and control; (b) uDCM_ij track uDCL**

The objectives of this voltage tracking scheme: 1) $u_{DCM\_ij}$ of all SMs sharing the same value as $u_{DCL}$, which means $u_{DCM\_ij}$ are balanced; 2) with the help from control loop maintaining the average value (which is balance value at the same time if 1) provided) of $u_{DCM\_ij}$ as $u_{DCM}*$, this scheme maintains $u_{DCL}$ as $u_{DCM}*$; 3) given turns ratio 1:1, same voltages of $u_{DCM\_ij}$ as $u_{DCL}$ guaranteed by fast response of DAB bring larger ZVS zone and less losses[4]; 4) because of the three-phase symmetrical system behavior, $u_{DCL}$ is kept horizontal, then tracking $u_{DCL}$ means making $u_{DCM\_ij}$ horizontal, and with suppressed ripples, MV dc link capacitors can be reduced.

## III. IMPROVEMENTS FOR VOLTAGE TRACKING CONTROL

As shown in Fig.5, to suppress the peak and bias of DAB inductance current, a pre-step phase shift (PSPS) method is applied, in which $i_{Lk}$ is the current through equivalent leak inductance $L_k$.

In each submodule, the single-phase line frequency AC output cause twice the line frequency voltage ripples at MV dc links, causing more losses and lower AC current quality. To suppress the MV dc link voltage ripples, different from conventional method of larger capacitors, it is proposed in [10] that, with reduced MV dc link capacitors, the reactive power from each MV ac phase is fed forward to the phase shift modulations (PSM) of corresponding DABs.
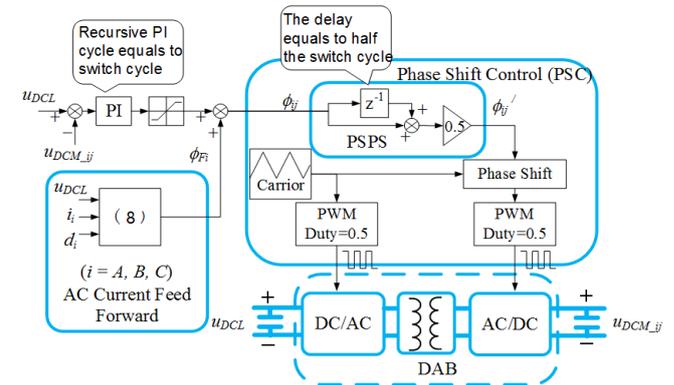


**Figure .5. Improvements for the voltage tracking control**

The sample of AC output current is fed forward to PSM of DAB to achieve fast dynamic response in this section, which helps deliver rippling power from MV dc link to LV dc link so that flat MV dc link voltage ($u_{DCM\_ij}$) can be expected. Three symmetrical flow of single-phase rippling power are collected into a common LV dc link and the collection doesn't ripple, making $u_{DCL}$ flat if PV input changes slowly. Derived from (5), the fed forward phase angle $\Phi Fi$ is calculated as (8), and submodules in a same phase share same $\Phi Fi$.

$$\dot{\phi}_{Fi} = \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2\pi^2 f_{zw} L_k d_i i_i}{u_{DCL}}}$$

(8)

## IV. SIMULATION RESULTS

### A. Grid Side Current and Average Voltage of MV dc links

In Fig.6 (a), AC current dynamics perform well when load switches, and unit power factor achieved, and regulations of id iq work normally; In Fig.6 (b), average voltage of MV dc links and voltage of LV dc link track each other well.

**Table.1. Simulation parameters**

| Line-to-line voltage | Grid side reactor in each phase | Equivalent leakage inductance in DAB | Rated power of single SM | Rated input DC current |
|---|---|---|---|---|
| 10kV/3 | 14mH | 181.6uH | 14kW | 210A |
| H-bridge switch frequency | Turns ratio of DAB transformer | Number of SMs in each phase | DC link voltage reference | Default MV dc link capacitor |
| 1.25kHz | 1:1 | 4 | 800V | 1.815mF |
| Overall rated power | Rated output AC current | DAB switch frequency | | |
| 168kW | 58A | 5kHz | | |

**(a)**
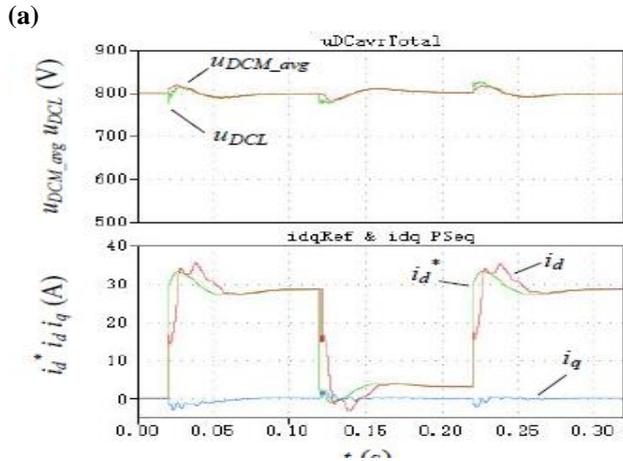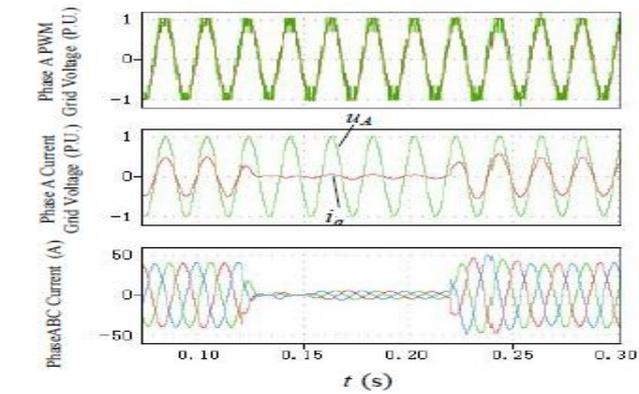


**(b)**

**Figure.6. Evaluation of overall control scheme. (a) AC current dynamic perform; (b) average voltage of MV dc links and voltage of LV dc link.**
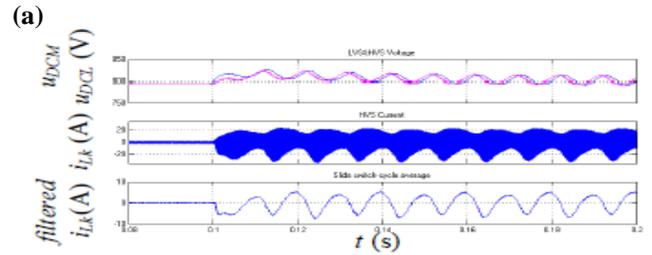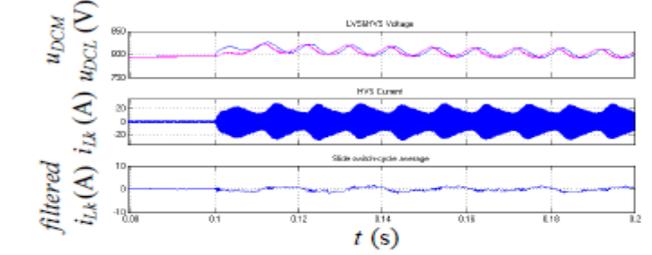


**(a)**
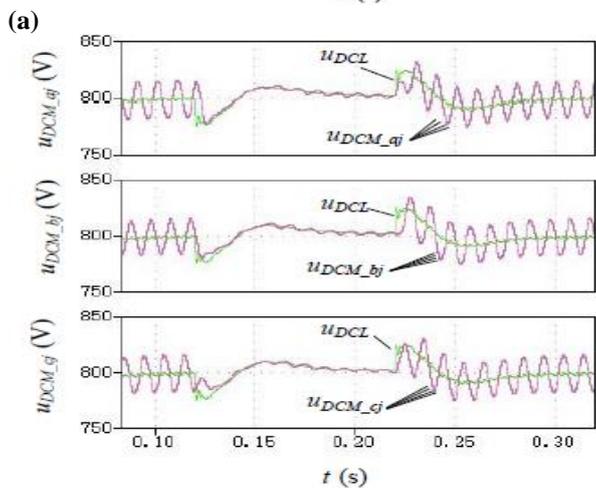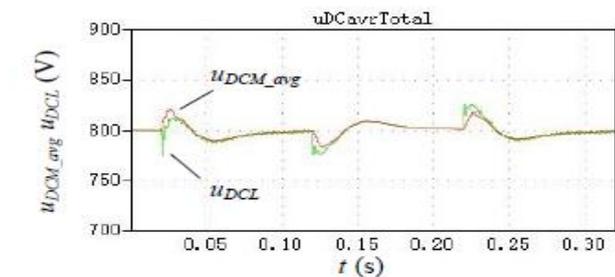


*(b)*

**Figure 7. Verification of voltage tracking and volatge balance of MV dc links. (a)average MV dc link voltage; (b) MV dc link voltage in each submodule**

## B. Voltage of All MV dc links and LV dc link

As figured in Fig.7(a,b), voltage of LV dc links track each other well, despite twice line frequency ripples.

## C. Validation of Pre-Step Phase Shift (PSPS) method

Compared with Fig.8(a), with pre-step phase shift, lower current peak and less flux storage for smaller fundamental component and lower loss are achieved.



**(a)**



**(b)**

**Figure .8. Effect of DAB pre-step phase shift. (a) without pre-step method; (b) with pre-step method**

## D. AC output current fed forward to the phase shift modulations (PSM) of DAB

With the feed forward, as in Fig.9, when load switches, dynamic responses are faster, and the MV dc link voltage ripples are suppressed. $uDCM\_ij$ balance is still achieved in Fig.9 (a, b).



**(a)**
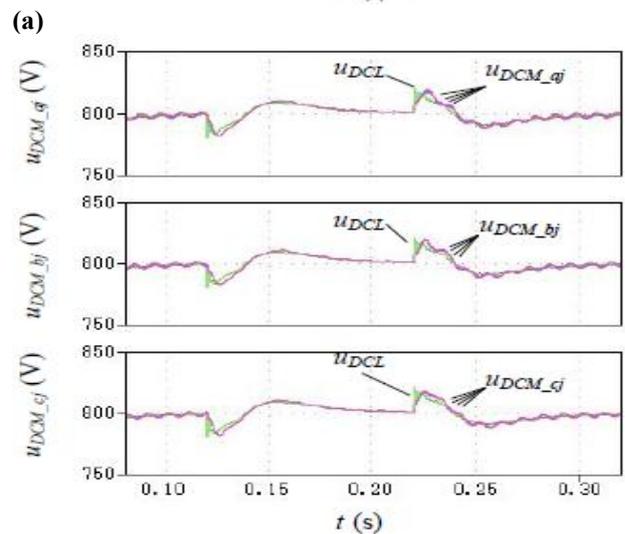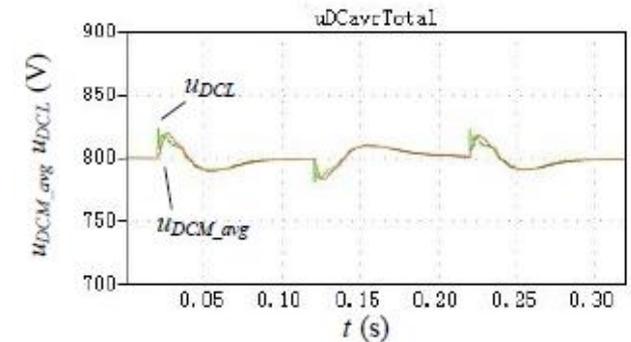


**(b)**

**Figure.9. Verification of voltage tracking and volatge balance of MV dc links when AC current feed forward method is applied. (a)average MV dc link voltage; (b) MV dc link voltage in each submodule.**

It is shown in Fig.10 that when MV dc link capacitors are reduced from the default of 1.815mF to 0.2 times of default AC current still performs well; the voltage ripples of MV dc link increase to acceptable peak-to-peak voltage of 30V as in Fig.11.
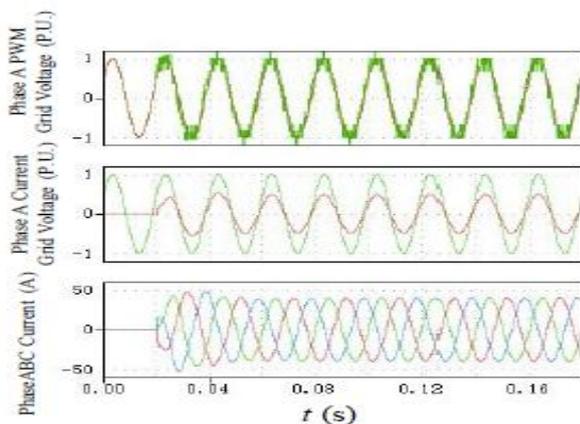


**Figure .10. The AC current with reduced capacitors of MV dc links and the AC current feed forward method applied.**
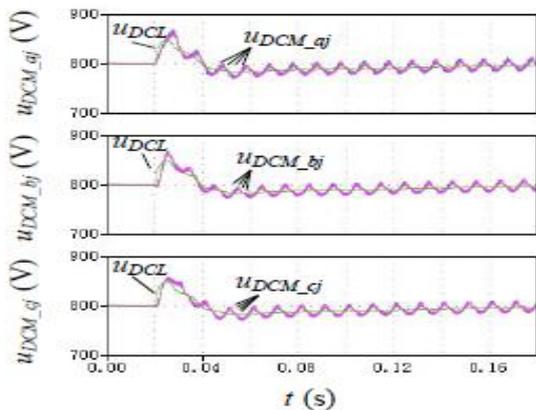


**Figure.11. the voltage of MV dc links with reduced capacitors of MV dc links and the AC current feed forward method applied.**

## V. CONCLUSION

In this paper, the voltage tracking control scheme of MV dc links in [8] is extended from single-phase SST for control of three-phase SST with improvements, and together with the control of an overall control scheme is proposed. With the organized tracking control of voltage of dc links, voltage balance of the SST is achieved, and the LV dc link is well regulated for PV plugin. Tracking control of voltage of MV dc link is improved, DAB current is shaped, and MV dc link ripples are suppressed. As the MV dc link ripples suppressed, capacitors can be smaller, better for a compact design of SST, but DAB current ripples increase, leaving the trade-off to be analyzed.

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