ISSN XXXX XXXX © 2018 IJESC

Research Article Volume 8 Issue No.11

Modified Half-bridge and Full-bridge Topologies with Continuous Input Current by using Switch-Boost Inverter

N.K.Rayaguru[1], K.N.HemanthKumar Teja[2]
Associate Professor[1], PG Scholar[2]
Department of Power Electronics
Vel Tech Rangarajan Dr.Sagunthala R&D Institute of Science and Technology, India

Abstract:
In this Modified half-bridge and full-bridge topologies with continuous input current by using switched-boost inverter are proposed. In this paper, the operation of the proposed inverters in different operating modes is analyzed. In addition, these topologies have high boost factor in comparison with conventional types. The proposed topologies have continuous input current and can generate zero voltage level in output. Then, the values of inductors and capacitors are designed. Comprehensive comparison between the proposed and conventional topologies in terms of boost factor, number of elements and efficiency shows in the proposed inverters. Finally, to verify operation of the proposed topologies by simulation.

INTRODUCTION:

Z-source inverter (ZSI) and quasi Z-source inverter (QZSI) have been presented. In switched inductor cells have been used in conventional ZSI to increase voltage gain. In this topology based on cascaded switched inductor cells has been used, which is named L-Z-source inverter (LZSI). The switched inductor Z-source inverter (SLZSI) has improved the value of boost factor . All presented topologies in use many passive elements. Hence, to reduce the number of passive elements in conventional topologies, switched-boost inverter (SBI) has been presented. To improve and develop the characteristic of SBI, current-fed switched inverter (CFSI) has been presented. To increase the boost factor in CFSI, developed switched Z-source inverter (DSZSI) has been presented. All presented topologies utilize full-bridge inverter in their power circuits and also half-bridge inverter is possible. Half-bridge Z-source inverter (HBZSI) iS uses in two impedance networks (Z-networks). In for application in electrochemical and electroplating industry and so.

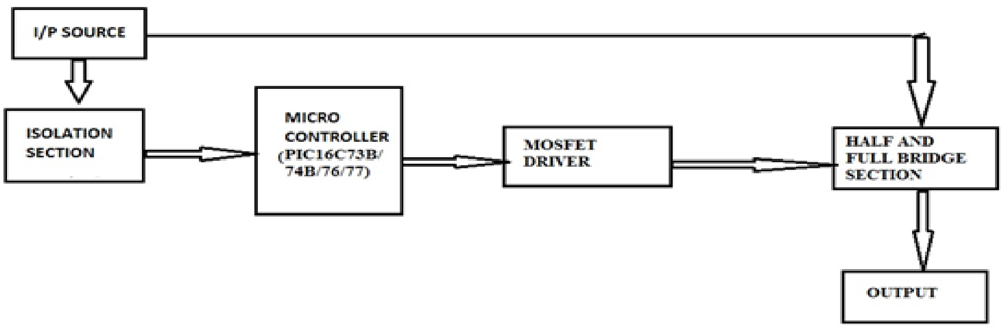
The proposed full-bridge inverter has eight operating modes. In the first and fifth operating modes, all switches S1,S2,S3 and S4 are ON. So, the proposed full-bridge inverter is in ST state. In other operating modes, only one of the switches on each leg is ON. So, the proposed full-bridge inverter is in nST state. The analysis of proposed half -bridge inverter is very similar to analysis of proposed as full-bridge inverter. The value of boost factor in full-bridge inverter is equal but voltage stress on capacitors has been decreased by 50% to value of boost factor in half-bridge inverter. It is noticeable that by selecting low values for inductance and switching frequency and high value for output load, number of operating modes will be more than eight. In this state, waveform of output voltage in proposed full-bridge inverter loses its symmetry state.

The proposed inverters have only one voltage source and few passive elements, including one inductor and few capacitors. It is noticeable that the proposed half-bridge inverter has six diodes and three high-side switches that these numbers are more than some of the conventional topologies. The high-side switches of the proposed half-bridge inverter can be driven by using bootstrap technique. In a schematic for this purpose is shown. According to this figure, the current follows a specific path to charge the bootstrap capacitor for high-side driver. Hence, there is no need for expensive drivers.

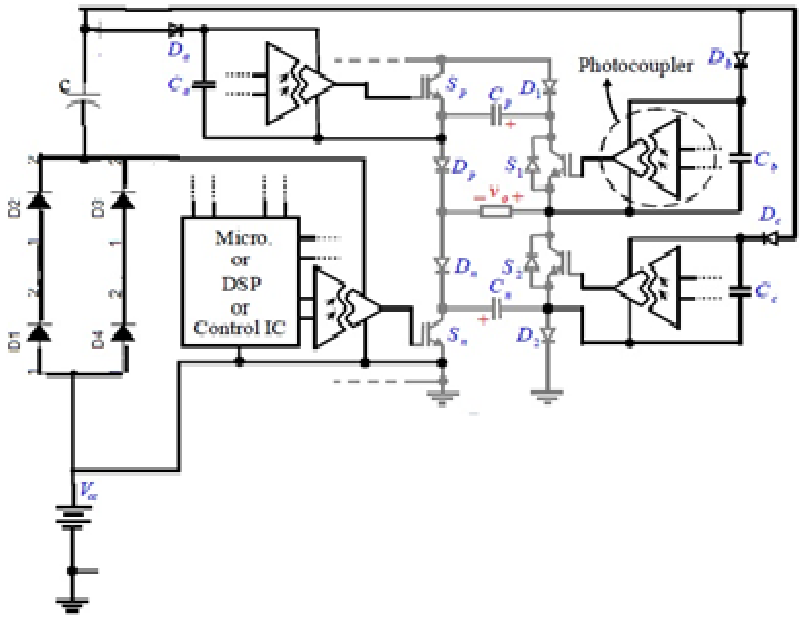
PROPOSED SYSTEM:

The proposed topologies have continuous input current and can generate zero voltage level in output. In this operation of the proposed inverters in different operating modes is analyzed. Then, the values of inductors and capacitors are designed as per required. Moreover, used switching pattern are used and to solve the above-mentioned limitations in conventional half-bridge and full-bridge inverters, topologies are proposed. In the proposed topologies the operation and functional principles of these topologies in different operating modes are discussed and coding are also used. Then, comparison between the proposed and conventional inverters is done. Finally, correct operation of the proposed inverters is verified by simulation in PSCAD/EMTDC software and experimental results.

BLOCK DIAGRAM:



CIRCUIT DIAGRAM:



OPERATIONAL MODES:

A. Operating Modes of the Proposed Half-Bridge Inverter

In the first operation, that is named synchronous operation of diodes (SOD), the diodes p D and n D are conducting simultaneously and are blocking simultaneously, too. In the second operation, that is named asynchronous operation of diodes (AOD), the diodes p D and n D are conducting simultaneously but these diodes are not blocking simultaneously. In SOD state, the proposed half-bridge inverter has four operating modes Duty cycles of switches 1 S and 2 S are named S 1 D and S 2 D , respectively. The trigger pulses S 1 G and S 2 G which are applied to switches 1 S and 2 S are similar and only have phase difference of 180 degree

1) First Operating Mode:

In the first operating mode, all switches are on and all diodes are off; hence, the inverter is in ST state. In this operating mode, voltage across inductor is positive; so, current through inductor (Li i) increases from its minimum value (1 I) to its maximum value (2 I). Moreover, stored energy in inductor increases.

The recent proposed inverter can generate zero voltage level in output.

2) Second Operating Mode:

In the second operating mode, switches 1 S and n S are on and switches 2 S and p S are off; hence, the proposed inverter is in nST state. In addition, diodes 1 D , p D and n D are on and diode 2 D is off. Voltage of inductor is negative; so, current through inductor (Li i) decreases from its maximum value (2 I) to its minimum value (1 I) and its stored energy decreases, as well.

3) Third Operating Mode:

In this operating mode, all switches of the proposed inverter are on; so, the proposed inverter is in ST state. In this operating mode the equivalent circuit of the inverter is similar to the mentioned equivalent circuit in the first operating mode.

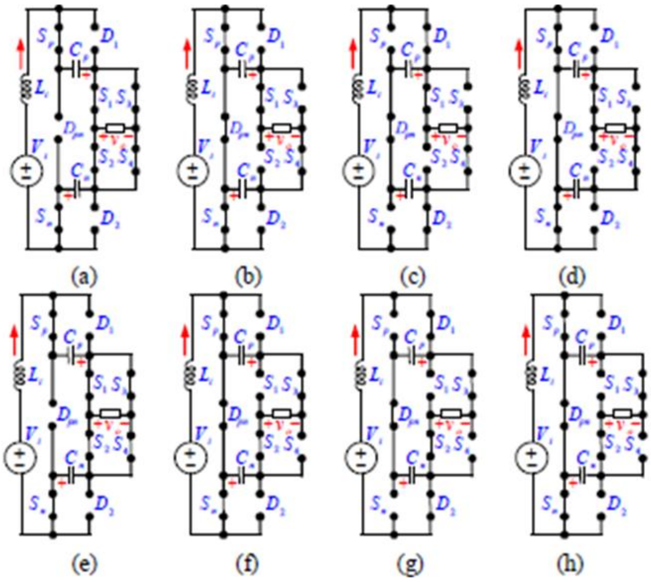
4) Fourth Operating Mode:

In this operating mode, 1 S and n S are off and 2 S and p S are on; so, the proposed inverter is in nST state. In addition, diodes 2 D, p D and n D are on and diode 1 D is off. By using KVL in this operating mode, load voltage is calculated.

In AOD, the proposed half-bridge inverter has six operating modes. In the first and fourth operating modes, 1 S and 2 S are on; so the proposed inverter is in ST state. In the second, third, fifth and sixth operating modes only one of the switches 1 S and 2 S is on; so, the proposed inverter is in nST state voltage and current waveforms of elements for the proposed inverter in AOD state.

B. Operating Modes of the Proposed Full-Bridge Inverter

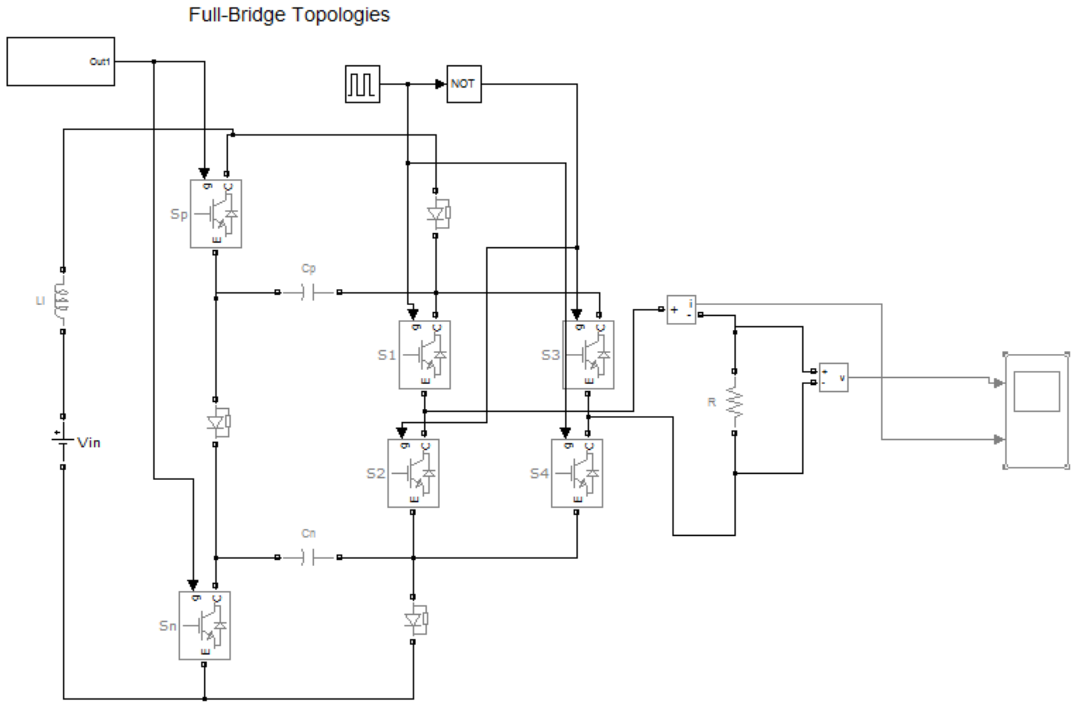
The proposed full-bridge inverter has eight operating modes which are shown. In the first and fifth operating modes, all switches 1 S, 2 S, 3 S and 4 S are on; so, the proposed full-bridge inverter is in ST state. In other operating modes, only one of the switches on each leg is on; so, the proposed full-bridge inverter is in nST state. The analysis of proposed full-bridge inverter is very similar to analysis of proposed half-bridge inverter; so detailed discussion about operating modes of the proposed full-bridge topology is not necessary. The value of boost factor in full-bridge inverter is equal to value of boost factor in half-bridge inverter but voltage stress on capacitors has been decreased by 50%. It is noticeable that by selecting low values for inductance and switching frequency and high value for output load, number of operating modes will be more than eight. In this state, waveform of output voltage in proposed full-bridge inverter loses its symmetry that is not appropriate.

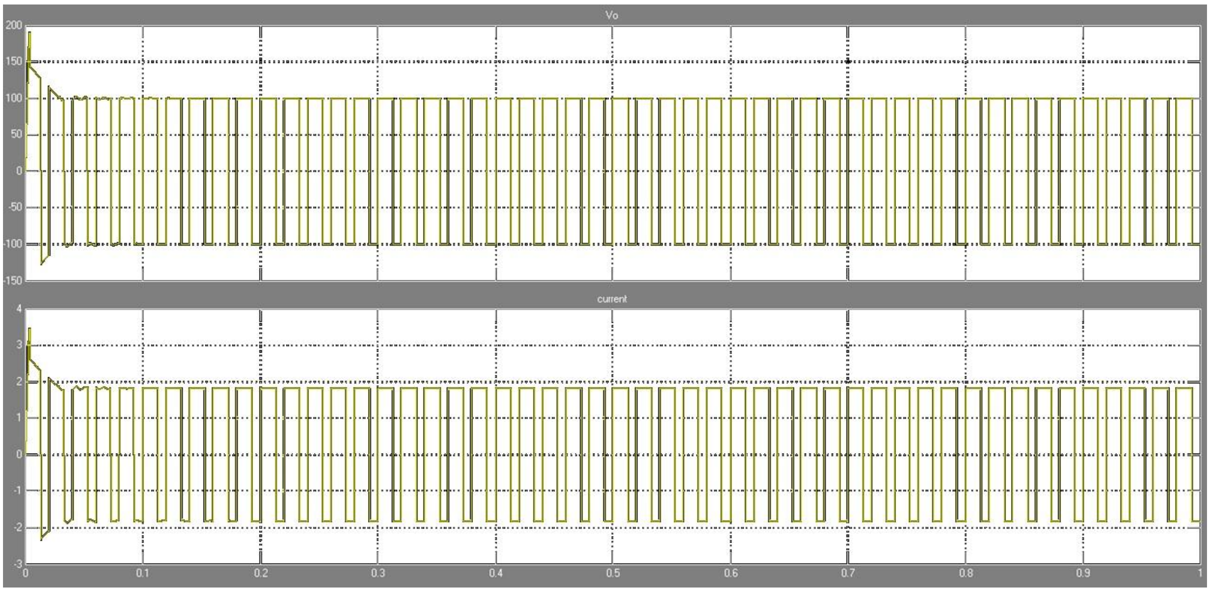


Equivalent circuits of the proposed full-bridge inverter in different operating modes

SIMULATION AND RESULTS

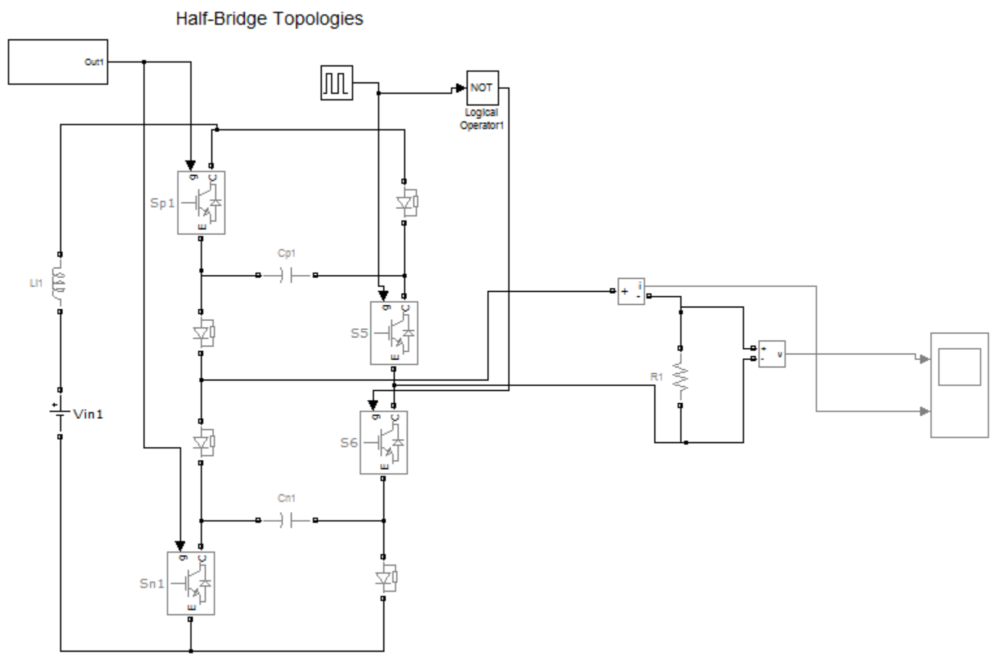
Full bridge converter:

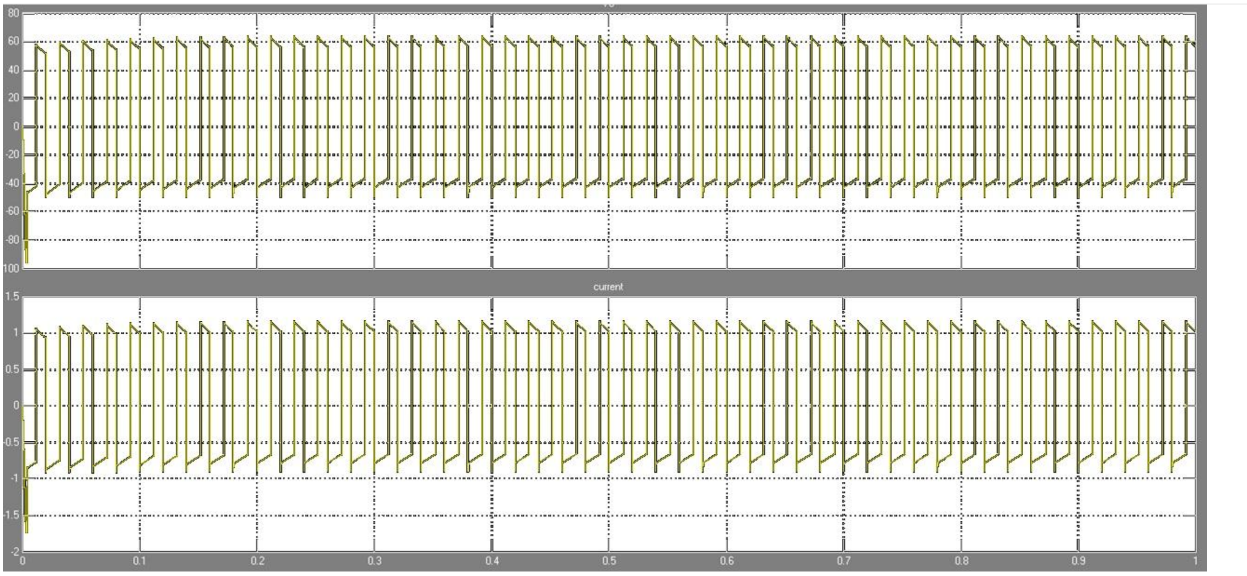




Result of full bridge topology simulation

Half bridge topology:





Results of half bridge topology simulation

CONCLUSION

In this thesis, Modified half-bridge and full-bridge topologies by using switch boost inverter were proposed and their different operating modes were discussed. Moreover, the values of voltage ripple of capacitors and current through inductor were calculated. These topologies have high voltage gain and high efficiency in comparison with conventional Z-source inverters. Other advantage of the proposed inverters is less number of passive components are used when compare to conventional Z source inverters. Moreover, the proposed inverters have continuous input current. The simulation results were reconfirmed the correct operations of the proposed topologies.

REFERENCE:

[1] Elias Shokati Asl , “New Half-Bridge and Full-Bridge Topologies for Switched-Boost Inverter with Continuous Input Current” vol: 65, no: 4, pp. 3188 – 3197, sep.2017

[2] F.Z. Peng, “Z-source inverter,” *IEEE Trans. Ind. Appl.*, vol. 39, no. 2,pp. 504–510, Mar./Apr. 2003.

[3] J. Anderson, F.Z. Peng, “Four quasi-Z-source inverters,” in *Proc. PESC*,2008, Rhodes, Greece, pp. 2743-2749.

[4] C.J. Gajanayake, F.L. Luo, H.B. Gooi, P.L. So, and L.K. Siow,“Extended-boost Z-source inverters,” *IEEE Trans. Power Electron.*, vol.25, no. 10, pp. 2642–2652, Oct. 2010.

[5] M. Zhu, K. Yu, and F.L. Luo, “Switched inductor Z-source inverter,”*IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150–2158, Jan./Feb.2010.

[6] D. Vinnikov, I. Roasto, R. Strzelecki, and M. Adamowicz, “Step-up dc/dc converters with cascaded quasi-Z-source network,” *IEEE Trans.Ind. Electron*., vol. 59, no. 10, pp. 3727–3736, Oct. 2012.

[7] L. Pan, “L-Z-source inverters,” *IEEE Trans. Power Electron.*, vol. 29,300 150 0 -150 -300 Vo [V] no. 12, pp. 6534–6543, Dec. 2014.

[8] A. Ravindranath, S.K. Mishra, and A. Joshi, “Analysis and PWM control of switched boost inverter,” *IEEE Trans. Ind. Electron*., vol. 60,no. 12, pp. 5593-5602, Dec. 2013.