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Time Composability of AMBA using AHB and APB Bridge Based on Memory Controller

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Abstract:
Microprocessor performance has improved recently these years. The increasing amount of logic that can be placed onto a single silicon die is driving the development of highly integrated SOC designs. An Advanced Microcontroller Bus Architecture (AMBA) compliant memory controller is designed for system memory control with the main memory consisting of SRAM, ROM and Dual port CACHE. The memory controller is the part of the system that, well, controls the memory. The aim is develop an architecture, design, and test AMBA AHB compliant Memory Controller for ARM based EMBEDDED platforms. Memory access time is reduced to a great extent by using AHB protocol thereby increasing the overall performance of the memory controller. We can access up to 32 APB slave peripherals APB bridge at a time in addition to that we increase the performance of the memory controller.

I. INTRODUCTION:

As the number and complexity of functions implemented in software in CRTES increases, achieving guaranteed high-performance is of paramount importance in all these markets. This has motivated the use of System-on-Chip architectures with high performance processor features including cache Memories and multicores (MPSoC).

AMBA is a high-speed, high-bandwidth bus that supports multi master bus management to get the most out of system performance. AMBA AHB bus which acts as the high performance system backbone bus for System on Chip applications is provided by ARM CPU.

AMBA is used in a wide range of architectures, providing flexibility in the implementation and backward-compatibility with existing AMBA interfaces. It has separate read and write data channels that provide low-cost Direct Memory Access (DMA).

It supports for issuing multiple outstanding addresses. It support for out-of-order transaction completion. It permits easy addition of register stages to provide timing closure.

The objective of AMBA specifications is to:

- Facilitate right-first-time development of embedded microcontroller products with one or more CPUs, GPUs or signal processors, are technology independent.
- To allow reuse of IP cores, peripheral and system macro cells across diverse IC processes.
- Minimize silicon infrastructure while supporting high performance and low power on-chip communication.
- Encourage modular system design to improve processor independence, and the development of reusable peripheral and system IP libraries

BLOCK DIAGRAM:

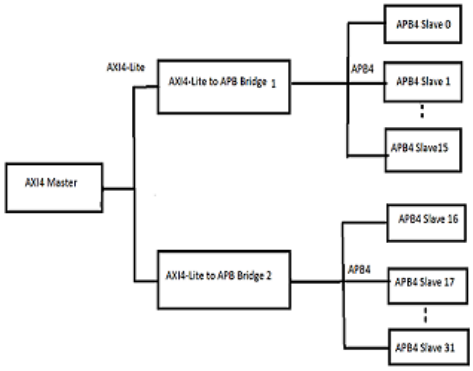


Figure.1. Block diagram:
The AXI4-Lite to APB bridge clock diagram is shown in Figure. The APB bridge provides an interface between the high-performance AXI domain and the low-power APB domain. It appears as a slave on AXI bus but as a master on APB that can access up to sixteen slave peripherals. Read and write transfers on the AXI bus are converted into corresponding transfers on the APB. Here, we are using two APB bridges one bridge can access up to (0-15) APB4 slaves and second bridge can access up to (16-31) APB4 slaves

ARCHITECTURE OF AHB-MC:

AHB is a new generation of AMBA bus which is intended to address the requirements of high-performance synthesizable designs.

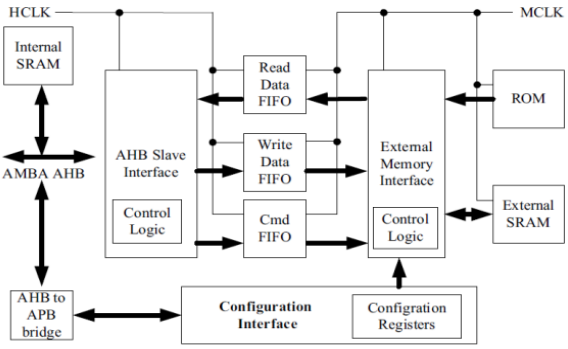


Figure.2. Architecture Of Ahb-Mc

It consists of five modules AHB slave interface, configuration interface, external memory interface, memory system, and data buffers.

i) **AHB slave interface:**

The AHB slave interface transfers the incoming AHB signal to the protocol used by the AHB-MC due to the complexity in the design some optimizations are made in the interface to improve performance. The AHB slave shown in figure maps the memory configuration space with the memory controller and performs the data transaction as AHB asserts its signal. It is a fully validated component so that it obeys both the internal protocol and AHP protocol.

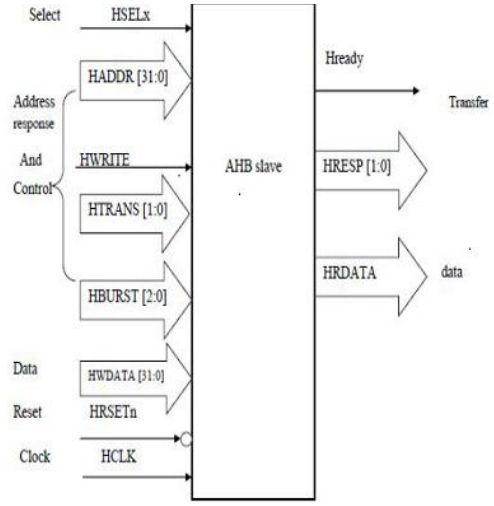


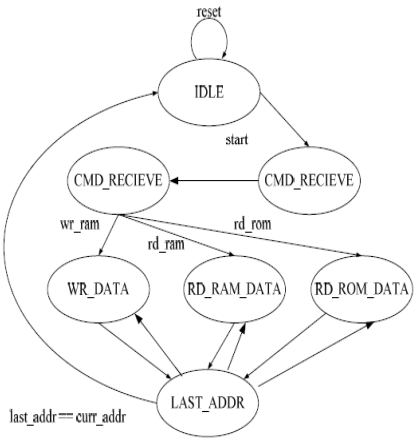
Figure.3.AHB slave interface

b)**CONFIGURATION INTERFACE:**

The main function of the configuration interface is to change the certain configuration registers according to the commands from AHB to APB bridge which converts AHB transfers from the configuration port to the APB transfers that the configuration interface require. It also provides the read and writes enable signals to the data buffers. The AHB configuration port is mapped to it using an AHB to APB Bridge.

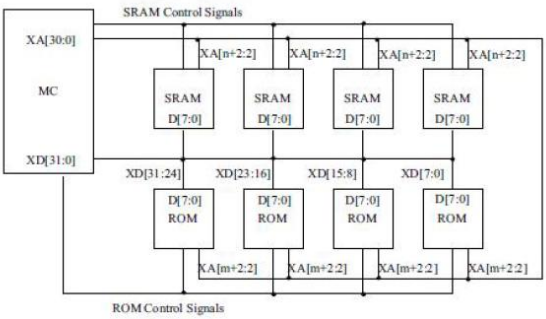
C) EXTERNAL MEMORY INTERFACE*:*

The external memory issues commands to thee memory from the command FIFO, and controls thee cycle timings of these commands. It generates the) Memory bank select and Memory write control signals.



d)**MEMORY SYSTEM:**

ARM architecture, instructions are all 32-bits, while instructions are 8-bits in the external ROM and SRAM. Therefore the lowest two addresses of ROM and SRAM are not connected to the external address bus. Additionally, to support byte writing, SRAM needs to be separated as four independent banks or has a byte-write enable signal. The basic memory system architecture.



e) **DATA BUFFER:**

To pass the data between clock domain is possible by most popular method FIFO.FIFO utilizes dual port memory for its storage one port is controlled by receiver and the other one is controlled by sender, which puts data into the memory as fast as data word per write clock.

AXI HANDSHAKE MECHANISM:

AXI 4.0 specification, in channel uses two signals for handshaking i.e., VALD and READY when the control information or data is available the source generate VALID signal whenever the receiver accept the control information or data by asserting READY signal. The below figure shows all possible cases of VALID/READY hand shaking. Note that when source asserts VALID, the corresponding control information or data must also be available at the same time the arrows in the figure indicate when the transfer occurs. A transfer takes place at the positive edge of the clock. Therefore source and destination use combinational circuit as output .In short, AXI protocol is suitable register input and combinational output circuit. The APB bridge buffers address, control and data from AXI4-Lite, drives the APB peripherals and returns data and response signal to the AXI4-Lite. It decode the address using an internal address map to select the peripheral. The bridge is designed to operate when the APB and the AXI4-Lite have independent clock frequency and phase. For every AXI channel, invalid comments are not forwarded and an error response generated. That is once an peripheral accessed does not exit, the APB bridge will generate DECERR as response to the response channel and if the target peripheral exists, but asserts PSLVERR, it will give a SLVEER response.

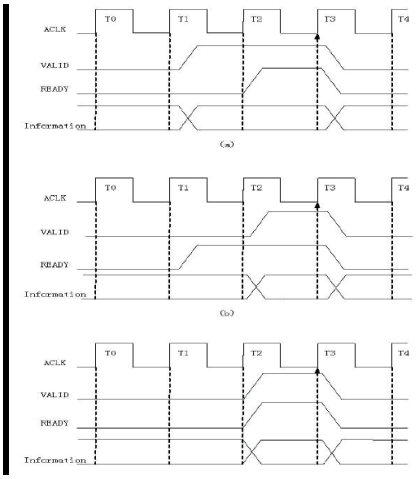


Figure.4.Axi Handshake Mechanism

ADVANCED PERIPHERAL BUS:

The AMBA APB is for low-power peripherals. AMBA APB is optimized for least power consumption and reduced interface complexity to support peripheral functions. APB can be used in conjunction with either version of the system bus.

BUS INTERCONNECTION:

The AMBA AHB bus protocol is considered to be used with a central multiplexor interconnection system. Using this method all bus masters drive out the address and control signals representing the transfer they wish to execute and the arbiter determines which master has its address and control signals routed to all of the slaves. A central decoder is also necessary to control the read data and response signal multiplexor, which selects the suitable signals from the slave that is implicated in the transfer. AHB is a new generation of AMBA bus which is proposed to address the requirements of high-performance synthesizable designs. It is a high-performance system bus that supports multiple bus masters and provides high-bandwidth operation. AMBA AHB implements the features required for high-performance, high clock frequency systems including.

- Burst transfers
- Split transactions.
- Single-cycle bus master handover
- Single-clock edge operation
- Non-Tristate implementation
- Wider data bus configurations (64/128 bits).

Bridging between this higher level of bus and the current ASB/APB can be done efficiently to ensure that any existing designs can be easily integrated. An AMBA AHB design may have one or more bus masters, typically a system would contain at least the processor and test interface. However, it would also be common for a Direct Memory Access (DMA) or Digital Signal Processor (DSP) to be included as bus masters.

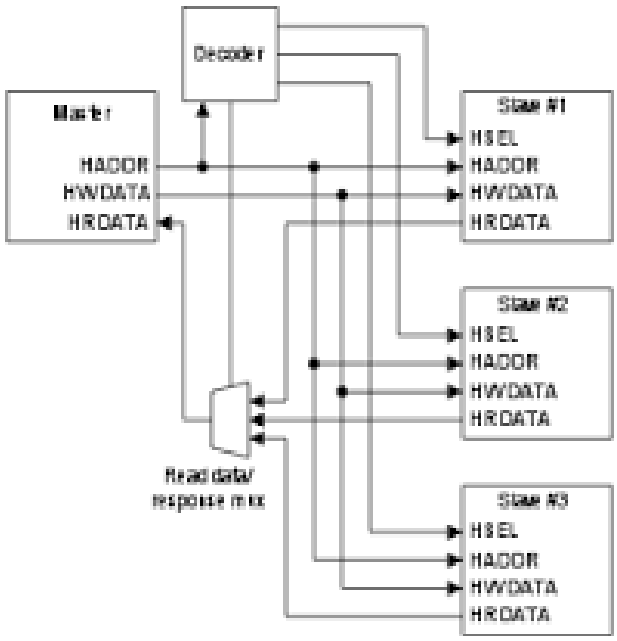
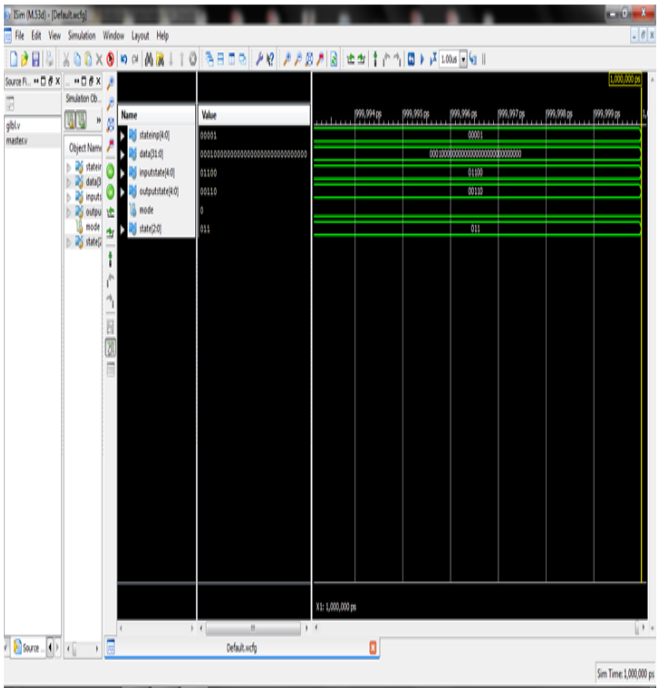


Figure.5. Bus interconnection

II. SIMULATION RESULTS:

In this figure we reduce the memory access time because the processor takes 8bits as one clock cycle and by using this AMBA processor it takes 32bits as one clock cycle. Hence the time period required for several processes is greatly reduced and by connecting 32 slave peripherals we are increasing the performance of the AMBA processor and by changing the state input the particular peripheral is only selected and the corresponding data also changes finally by this project we are increasing the performance accuracy of AMBA and minimizing the power consumption for the processes needed to be performed by the system. We are selecting only peripheral and controlling it for which data has to be READ after reading the data we perform WRITE operation and data is display in the simulation result. We are using five bit state input because of 32 slave peripheral that is (2^5=32) variation in any one of the five bit of the state input the peripheral is selected and the data goes to that particular slave and displayed on the output graph. The controller plays a key role and it processes the state input, data, input state, output state, mode state. Totally we are using seven slaves and the same action is for (16-31) peripherals because the same APB bridge. AXI is a specification in AMBA3 which only defines interfaces between the master and the slave, the master and the interconnect and the slave and the interconnect; allowing the chip designer to use potentially any interconnect. On the one hand, in order to determine whether time-compos able access delays for the interconnect can be achieved, a specific interconnect has to be defined and analyzed.



III. CONCLUSION:

In this thesis we observe that the data transfer operation from one memory to another memory is fast as compared to serial communication by proposing the parallel communication in AMBA AHB. It also provides the opportunity to use master and slave up to 16 no's and in extension we are using up to 32 slaves the data of every master is read and write simultaneously. Here AMBA AHB supports the data transfer by reducing the time and increases the frequency of the bus to increase the system performance. The use of high capacity memory management with the AMBA AHB in this thesis successfully attempted to find the software solution for the problem of memory compliant in the microcontroller. The proposed implementation is capable of running in any PC with Xilinx. This implementation able to sustain the external memory bandwidth, on which the CPU, on-chip memory and other direct memory access devices reside.

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