ISSN XXXX XXXX © 2018 IJESC

Research Article Volume 8 Issue No.4

Design of Low Power Booth Multiplier Based Reconfigurable FIR Filter for DSP Applications

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Abstract:
Recent advances in mobile computing and multimedia applications demand high-performance and low –power VLSI digital signal: processing (DSP) systems. One of the most widely used operations in DSP is finite-impulse response (FIR) filtering. In the existing method FIR filters is designed using array multiplier, which is having higher delay and power dissipation. The proposed method presents a programmable digital finite impulse response (FIR) filter for high-performance applications. The FIR filter performs the weighted summations of input sequences and widely used in video convolution functions, signal preconditioning, and various communication applications. Recently, due to the high-performance requirement and increasing complexity of DSP and multimedia application.

Index terms: Noise Reduction, Baugh-Wooley Multiplier, Booth-Recoded Multiplier, FIR filter, Xilinx, ModelSim.

I.INTRODUCTION

In this work, FIR filter multipliers are extensively characterized with power simulations, providing a methodology for the perturbation of the coefficients of baseline filters at the algorithm level to trade-off reduced power consumption for filter quality. The proposed optimization technique does not require any hardware overhead and it enables the possibility of scaling the power consumption of the filter at runtime. In our proposed system, we have developed Wallace multiplier to the radix-4 modified Booth multiplier.The graph shows the improvement,

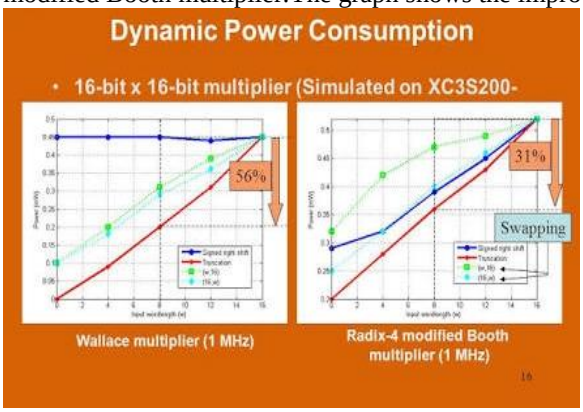

Figure.1.Power consumption of Wallace and booth multiplier.

VHDL used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits. VHDL can also be used as a general purpose parallel programing language.VHDL has constructs to handle the parallelism inherent in hardware designs, but these constructs differ in syntax from the parallel constructs in tasks.The key advantage of VHDL, when used for systems design, is that it allows the behavior of the required system to be described and verified before synthesis tools translate the design into real hardware.

II.EXISTING METHOD

The BW2 multiplier is a simple structure which can achieve medium operating speed with moderate silicon area. Two n-bit input operands are passed to the PPG that implements the Baugh-Wooley scheme, which feeds the PPR implemented as a carry-save adder with (m,2) compressors. For the considered implementation, the half adders and full adders instantiated inside each of the compressors are connected in a tree structure to reduce the critical path of the PPR.

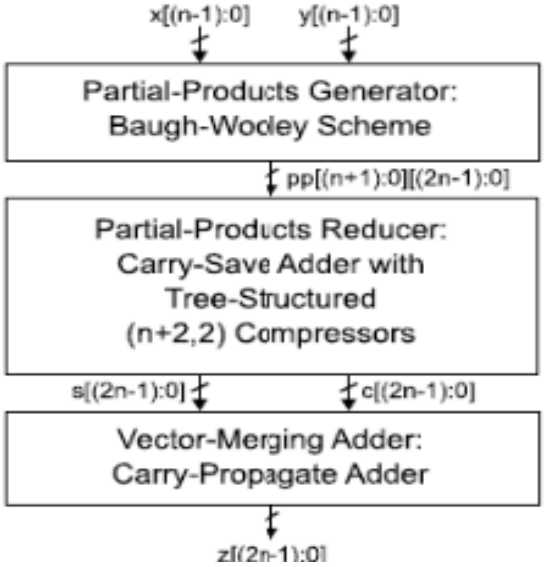

Figure.2. Block diagram of existing system.

For this reason, inorder to reduce the power consumption of the BW2 multiplier, we first analysethe switching activity of the implemented PPR

III.PROPOSED METHOD

This technique can be effectively be applied, as an example, to reconfigurable FIR accelerators.A simply greedy algorithm is used to modify the coefficients of a baseline filter to derive a new set of coefficents that are optimized for low power consumption while allowing for some degradation of the filtering quality.By exploiting the flexibility on the algorithm level,the proposed approximate computing technique does not require any design overhead for a programmable accelerator.At the same time,it ensures the quality of the baseline filter whenever it is required,while it offers also the possibility of scaling the power consumption at runtime when energy is short and reduced accuracy is tolerated.Since radix-2 Baugh-Wooley multipliers are rather slow, we also study a fast multiplier that uses Booth recoding.

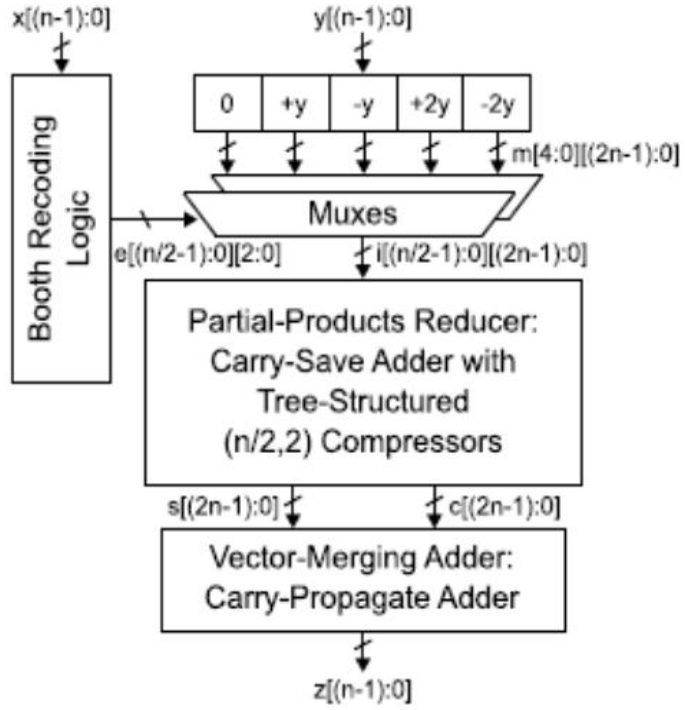

Figure.3. Block diagram of our proposed system.

A BR4 multiplier has been considered where the PPR is fed with less than half of the partial products of those in the BW2 multiplier, thereby providing a much shorter circuit path. As opposed to the symmetric BW2 multiplier, inthe BR4 topology, the two input operands are processed differently, since x is passed to the recoding logic that decides which multiplies of y should be fed to the PPR.For the considered implementation, a carry-save adder with (m,2) compressors is used for the PPR and a carry-propagate adder is used for the VMA,as in the BW2 multiplier.

A.Multipliers:

Multipliers play an important role in today'sdigital signal processing and various other applications.With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets- high speed, low power consumption, regularity of layout and hence less area are even combination of them in one multiplier thus making them suitable for various high speed,low power and compact VLSI implementation.

```
          0  1  0  1
          0  0  1  1
    ---------------
          0  1  0  1
       0  1  0  1
    0  0  0  0
 0  0  0  0
 ---------------
 0  0  0  1  1  1  1
```

The common multiplication method is "add and shift" algorithm.In parallel multipliers number of partial product to be added is the main parameter that determines the performance of the multiplier.Modified Booth algorithm is one of the most popular algorithms.

B. FIR FILTER:

In digital signal processing, an FIR is the filter whose impulse response is of finite period, as a result of it settles to zero in finite time. This is often distinction to IIR filters, which can have internal feedback and will respond indefinitely. The impulse response of an N+1 samples before it then settles to zero. FIR filters are most popular kind of filters executed in software and these filters can be continuous time, analog or digital and discrete time.

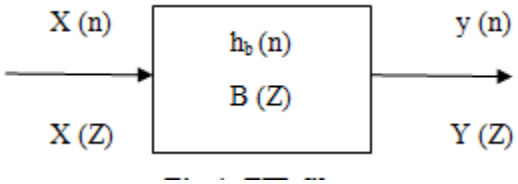

Figure.4. FIR filter

A filter requires more compotation time on the DSP and more memory. The DSP chip therefore needs to be more powerful. FIR filters are specified using a large array of numbers.The formulae for FIR filter is given by,

$\mathbf{Y[n]} = \sum_{k=0}^{N-1} \boldsymbol{h[k].x[n-k]}$

FIR filter can implement linear-phase filtering. This means thus the filter has no phase shift across the frequency band. The architecture of the FIR filter was designed by,

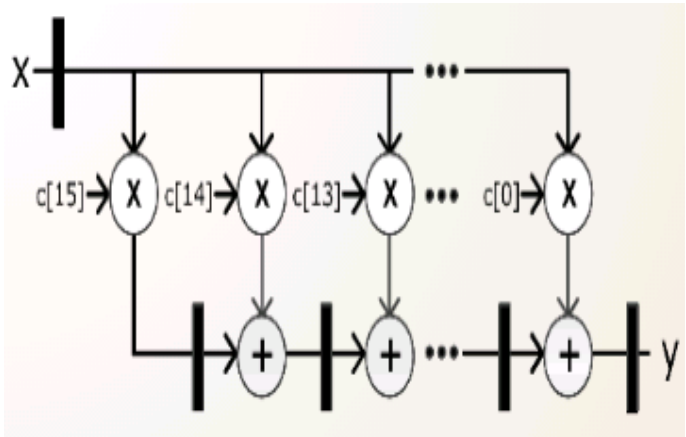

Figure.5. Architecture of FIR filters.

C. BAUGH-WOOLEY MULTIPLIER:

By understanding the Baugh-Wooley multiplication algorithm for 2's complement data, the two n-bit input operands are passed to the PPG that implements the Baugh-Wooley scheme which feeds the PPR implemented as a carry save adder with compressors. Each compressor have the half adder and full adder. The compressors are connected in a tree structure to reduce the critical path of the PPR.The PPR consumes large amount of power. For this reason, in order to reduce the power consumption of the BW2 Multiplier, we first analyse the switching activity of the PPR.

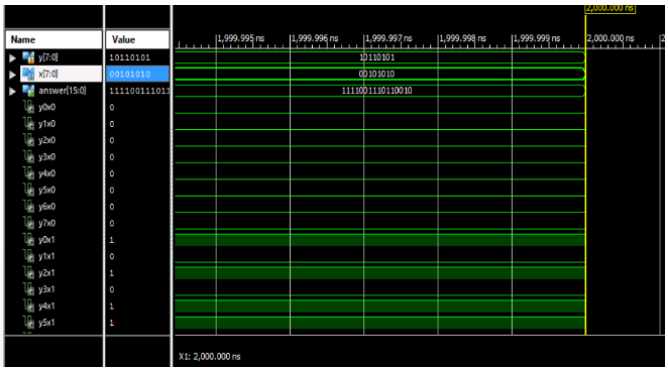

Figure.6. Simulation output for Baugh-wooley

D. RADIX-4 BOOTH MULTIPLIER:

Radix-2 Baugh-Wooley multipliers are rather slow; we also study a fast multiplier that uses booth recoding. In this method PPR is fed with less than half of the partial product of those in the BW2 Multiplier, thereby providing a much shorter critical path. For the considered implementation, a carry-propagate adder is used for the PPR and a carry-propagate adder is used for the VMA, as in the BW2 multiplier.

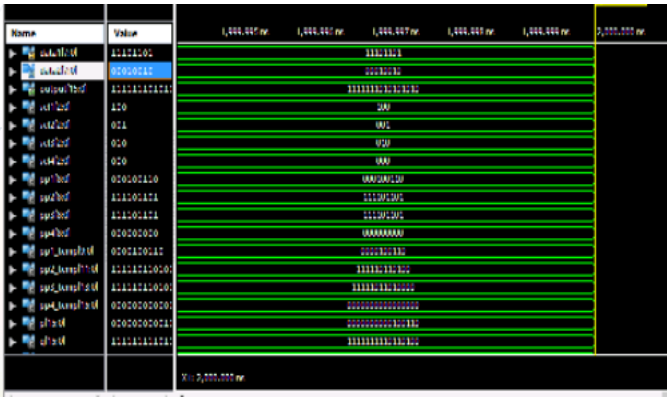

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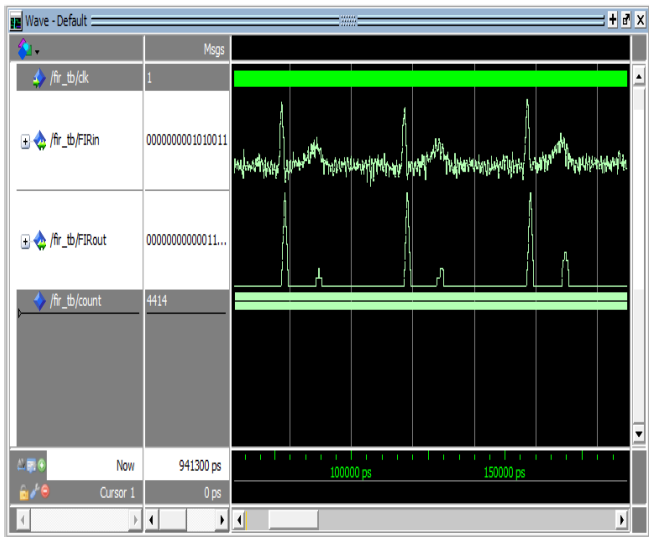
Figure.7. Simulation output for Booth multiplier

In BR4 topology it presents a more complex structure than BR2 PPG as it includes both the Booth recoding X AND Y. They are essential to obtain a better estimation of the multiplier power consumption.

IV. EXPERIMENTAL SETUP

Thus our proposed method reduces the time delay ranges from 32.153 ns to 23.724ns by the Baugh-Wooley multiplier and the power ranges from 0.224 watts to 0.223 watts by the Booth recoding multiplier.



V. CONCLUSION

By our proposed system, wegives a clear concept of 8*8 Baugh-Wooley multiplier and Booth multiplier and their implementation in low power dissipation and reduces time delay. We found that 8*8 Baugh-Wooley multiplier aremuch option than the Conventional multiplier. We concluded this from the result of Power Consumption and Time Delay.

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