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A Review of High Gain Single Stage Boosting Inverter for Photovoltaic Applications

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Abstract:
This paper introduces a review of high-gain single-stage boosting inverter (SSBI) for photovoltaic applications .The two-stage micro inverter first performs dc to dc voltage step up and then converts dc to ac, whereas the single-stage topology has to perform the dc to dc voltage step up, and the dc to ac conversion functions all in one stage. This paper discusses about various previous conventional single stage boosting inverter topologies as well as the proposed single stage boosting inverter topology. The proposed system employs a Tapped Inductor to attain high-input voltage step up and, thus, allows operation from low dc input. The conventional methods are costly and has complex circuitry whereas the proposed Single stage boosting inverter has a simpler circuitry and a lower component count. The proposed Single stage boosting inverter can achieve high dc input voltage boosting, good dc–ac power decoupling, good quality of ac output waveform, and good conversion efficiency.

Keywords: Micro inverter, one cycle control (OCC), tapped inductor TI.

1. INTRODUCTION

The interest in using renewable energies has grown significantly in the recent yearsfrom both the industries and governments all over the world due to their environmental friendliness and also due to the depletion of fossil fuels. Among renewable sources, the photovoltaic (PV) has witnessed the unprecedented growth. Within PV systems, power inverters are required to inject the PV power into the ac grid. Micro inverter topologies for photovoltaic (PV) power generation are classified into three major groups the single-stage, the two-stage, and the multi-stage types. The multistage micro inverters are usually comprised of a step up dc–dc converter front stage, an intermediate high-frequency dc– dc converter stage, used to attain a rectified-sine waveform, and a low frequency unfolding stage to interconnect to the grid .However, the multistage converter requires more number of components and is very costly to implement. The two-stage micro inverter first performs dc to dc voltage step up and then converts dc to ac, whereas the single-stage topology has to perform the dc to dc voltage step up, and the dcto a c inversion functions all in one stage. In order to convert and connect the solar energy to the grid, the low voltage of the PV panel first has to be stepped up significantly to match the utility level. This poses a challenge to the designer of PV inverters as the traditional boost converter cannot provide the required gain at high efficiency. To overcome this problem single stage boosting inverter is used which can attain higher dc gain and the power decoupling is performed at high voltage; hence, low value of dc-link decoupling capacitor is required. But there are several topologies of single stage boosting inverter which are discussed in this paper out of which the proposed single stage boosting inverter has several advantages over other old conventional SSBI topologies. The Proposed SSBI is discussed in detail which uses one cycle control (OCC), which helps attaining High -quality ac output regardless of low frequency rippleacross the dc link.

2. PREVIOUS SSBI TOPOLOGIES

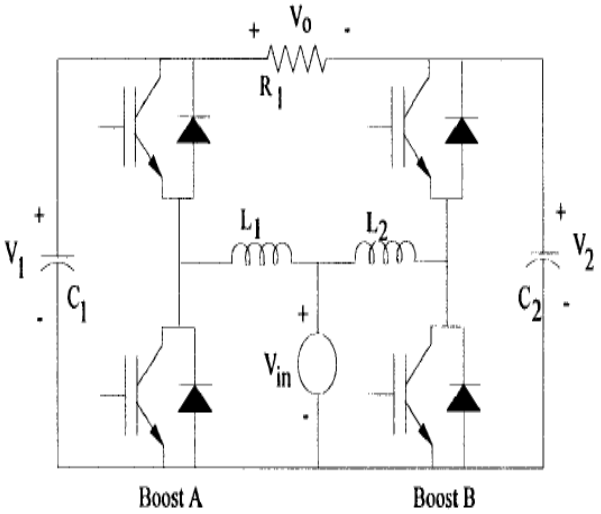

Figure.1. Topology presented in [2]

The topology presented in [2] uses a dual boost inverter. Here, the load is connected differentially between the outputs of two bidirectional boost converters as shown in Fig 1. As a result, the topology resembles acommon *H*-bridge with the boosting inductors connected to the leg midpoint. The disadvantages of this approach are the limited dcStep-up gain; circulating currents, which reduce the efficiency; and complicated control. Since the function of capacitor *C*1 and *C*2 is output filtering, the decoupling capacitor should be placed at the low voltage input, which is another disadvantage.

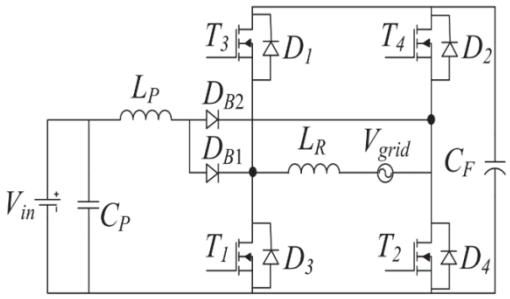

Figure. 2. Topology presented in [3]

The topology presented in [3] use a single boost inductor; have no circulating currents; have a high voltage dc link and, thus, a smaller decoupling capacitor as shown in Fig.2. But the limited dc step up of [3] necessitates using a more expensive high-voltage PV panels in order to get desired dc-bus voltage compatible to grid connected inverters.

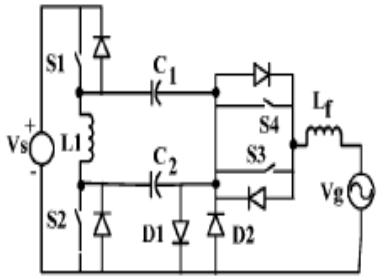

Figure.3. Topology presented in [4]

The topology presented in [4] is derived from basic zeta configuration and is shown inFig. 3. This is an improved configuration as it uses minimal number of devices and does not have the drawbacks of simultaneous, high frequency operation of all the switching devices. In the positive half cycle of the grid voltage, S1 operates at high frequency while S2 and S4 are kept ON. Power transfer during this period is based on the buck-boost principle. Similarly, during the negative half cycle, S2 is operated at high frequency while S1 and S3 are kept continuously ON. Power transfer during this period follows the boost principle as source is active during both the ON and OFF intervals. This leads to asymmetrical operation of the converter in the two halves of the grid cycle, which is a major drawback of this system because it requires a complex control strategy to prevent dc current injection into the grid. The main advantage of this configuration is that it has low switching losses.

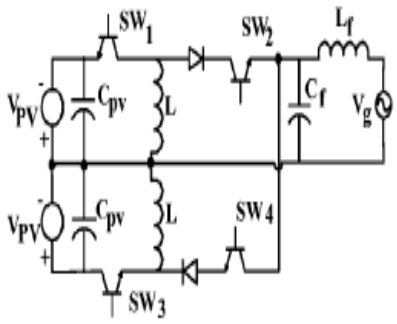

Figure.4. Topology presented in [5]

The topology presented in [5] is based on a half-bridge buck-boost inverter configuration, as shown in Fig. 4. This configuration eliminates the drawback of asymmetrical operation during the two half cycles of a grid voltage. It is a good configuration because it has minimum switching and conduction losses because only two devices are used during any half cycle of the grid voltage. Since a minimum number of switches are operated at high frequency so it has less EMI concerns and high reliability. The drawbacks with this configuration, however, are that it uses a pair of PV sources only one of which is utilized in a given half cycle of the grid voltage. High value of filter capacitor across each of these PV sources is required.

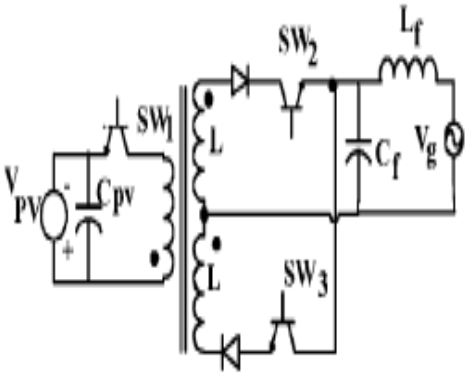

Figure.5. Topology presented in [6]

The topology presented in [6] is based on isolated fly back configuration as shown in Fig. 5 which is a modification of the half bridge buck- boost topology shown in Fig. 4 .This topology uses only three power devices and an isolation transformer. It also uses the buck-boost principle. This is a good scheme, but there are additional losses due to the transformer, though it provides isolation between the PV and grid sides.

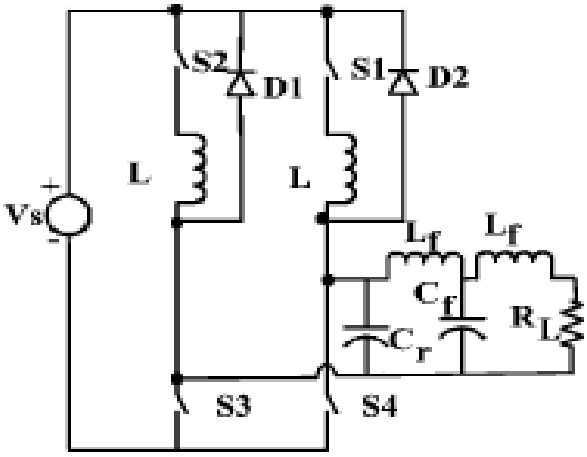

Figure.6. Topology presented in [7]

The topology presented in [7] is a single-stage, full bridge configuration based on the buck-boost principle as shown in Fig. 6. During the positive half cycle of the grid voltage, switch S4 operates at high frequency and S1 is kept continuously ON. The path during turn OFF is completed through S1 and D2. During the negative half cycle of the grid voltage, S3 operates at high frequency and S2 is kept continuously ON. During turn OFF, the path is completed through S2 and D1. This configuration has a large number of devices conducting at a given instant which result in higher conduction losses.

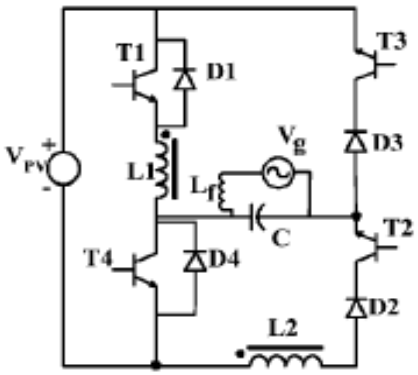

Figure.7. Topology presented in [8]

The topology presented in [8] is based on the buck-boost principle as shown in Fig. 7. This topology uses fly back principle with mutually coupled coils during the negative half cycle of the grid voltage. The limitation of this system is that it can be used only for low power applications. In addition to this, the switching and conduction losses are higher and the operation is asymmetrical in the two halves of the grid voltage cycle.

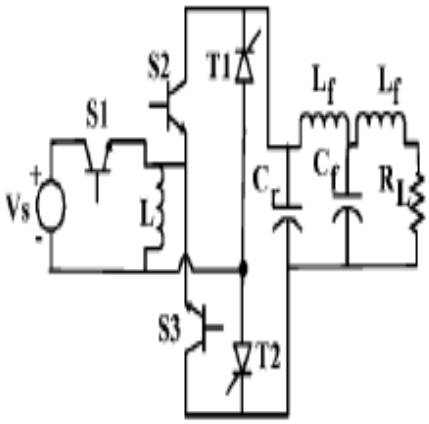

Figure. 8. Topology presented in [9]

The topology presented in [9] is another single-stage configuration based on buck-boost principle as shown in Fig. 8. Though this configuration is not specifically intended for grid connected PV systems, it may be considered for this application. But the drawback with this configuration is that it uses five switches, with three switches operating at high frequency, leading to EMI problems and higher switching losses.

3. PROPOSED SSBI TOPOLOGY

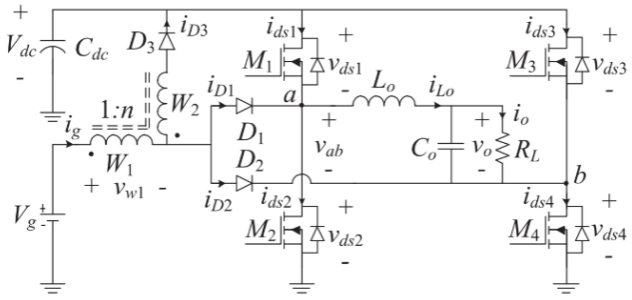

Figure. 9. Topology of the proposed SSBI [1]

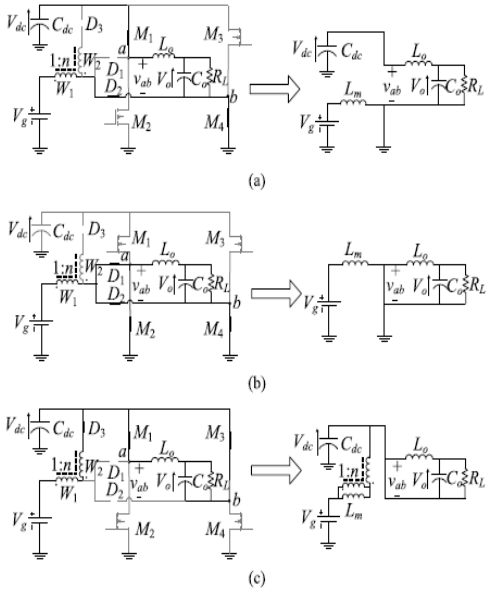

Figure.10. Topological states of the proposed SSBI [1]

The schematic diagram of the proposed SSBI [1] is given in Fig. 9. SSBI is comprised of four semiconductor switches M1, M2, M3 and M4 arranged in a full-bridge configuration; steering diodes D1, D2 ; dc-linkdiode D3 , the tapped inductor (TI) W1:W2; the decoupling capacitor C dc; and the output filter Lo − Co. The load is represented by the resistor Rl.The proposed SSBI is supplied by a dc voltage source, Vg obtained from single PV panel, and generates ac output voltage V o .Here, the input current is considered as Ig the output current is ioand its average component is Io. Compared to conventional methods the proposed SSBI topology has the advantages of a larger voltage step up which can be achieved adjusting the Tapped Inductor turns ratio, and smaller decoupling capacitor, which is placed on high voltage dc bus. Principle of operation of the proposed SSBI is dependent on implementation of a specialized switching pattern of the h bridge. For generating output of positive polarity, three topological states are created during the switching cycle as shown in Fig.10.In order to generate output voltage of negative polarity, complementary switching states are created by the controller.

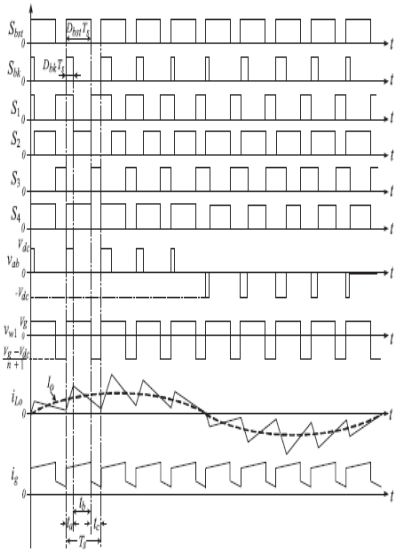

Figure. 11. Key waveforms of the proposed SSBI [1]

The switching cycle starts with State A, shown in Fig. 10 which lasts for a duration of t a. Here, the switches M1 and M4 are ON, whereas switchesM2 andM3 are OFF, D2 conducts and D1, D3 are cut-off. During this state, the TI primary magnetizing inductance Lm is charged from the input voltage source V g, while the dc voltage V dc is applied to the input terminals of the output filter so the filter inductance Lo is charged feeding also the filter capacitor Co and the load R l . State B begins, as the switchM1 is turned off and M2 is turned on, whereas M4 keeps conducting. State B lasts for a duration of t b .Here, both D1 and D2 conduct while D3 is cut-off. As a result, the TI magnetizing inductance Lm continues charging from the input voltage source V g, whereas the input terminals of the output filter are shorted so the filter inductance Lo is discharged to the output capacitor Co and the load R l.State C begins as the switches M1, M3 are turned on and M2, M4 are turned off. State C lasts for duration of t c, and completes the switching cycle. Here, both D1, D2 are cut-off and D3 conducts; the TI magnetizing inductance Lm is discharged via both windings and D3 into the dc-link capacitor C dc, while the input terminals of the output filter are shorted and the filter inductance Lo feeds the output capacitor Co and the load Rl.Key waveforms of the proposed SSBI [1] throughout a line frequency cycle are illustrated in Fig. 11.

4. CONCLUSION

A review of several high gain single stage boosting invertersis presented in this paper. It can be seen that proposed single stage boosting inverter has several advantages over other conventional single stage boosting inverter topologies.The proposed single stage boosting inverter has a simpler topology and a lower component count. The proposed SSBI can achieve high dc input voltage boosting, good dc-ac power decoupling, good quality of ac output waveform, and good conversion efficiency. The proposed SSBI topology has the advantage of high voltage stepup which can be further increased by adjusting the Tapped Inductor turns ratio. The ac - dc power decoupling is attained on the high-voltage dc link and therefore requires a relatively low capacitance value.

5. REFERENCES

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